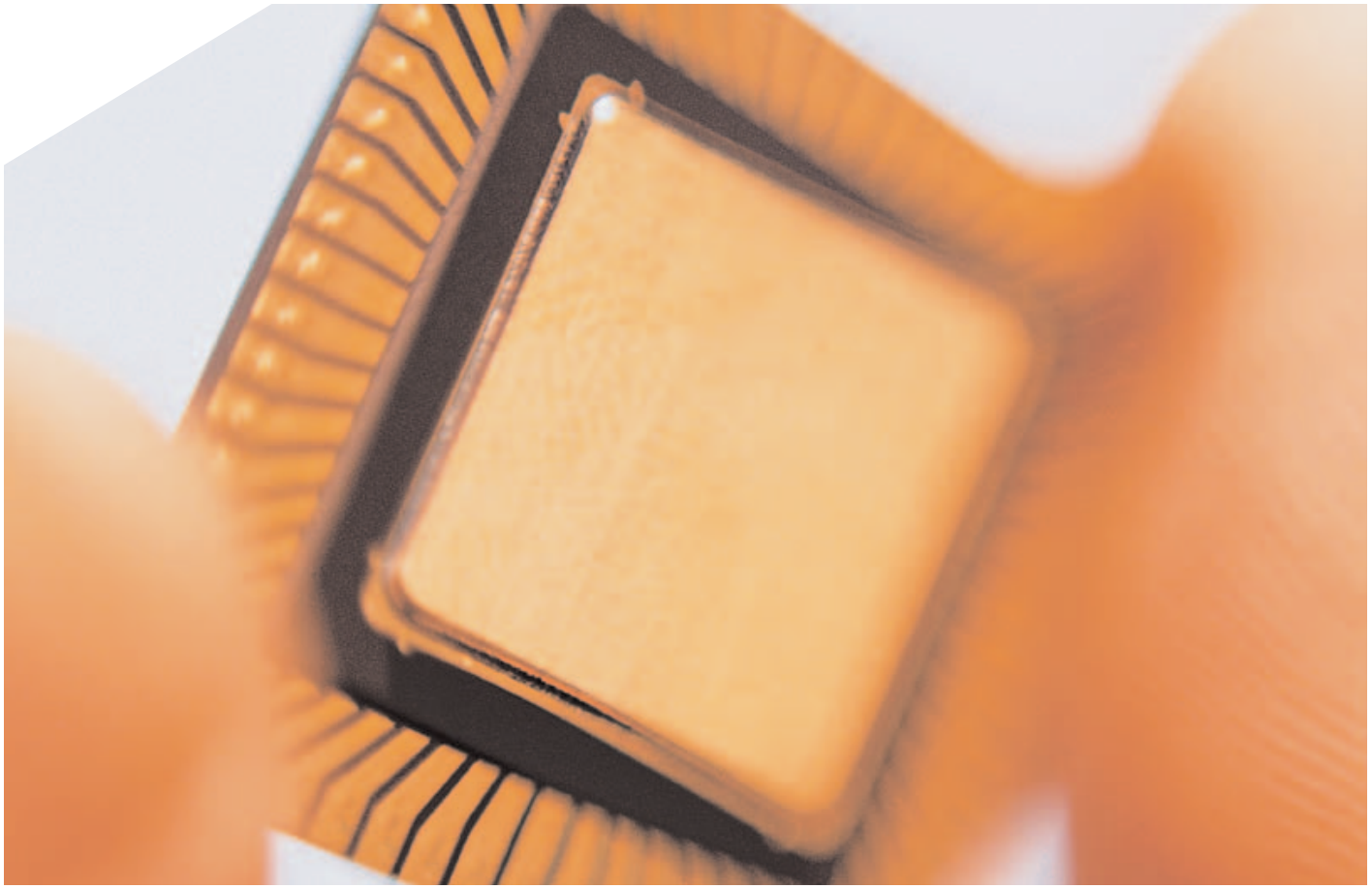
Product Catalog



Semiconductor Intellectual Property & Technology Licensing Program

Launched by Motorola
freescale semiconductor

MANUFACTURING PROCESS TECHNOLOGY OVERVIEW

	90 nm	130 nm	0.18 µm	0.25 µm	0.35 µm	>0.40 µm
Logic	CMOS—SOI CMOS—general purpose* CMOS—low power*	CMOS—SOI CMOS—general purpose CMOS—low power	CMOS—SOI CMOS—general purpose CMOS—low power	CMOS	CMOS	–
SMARTMOS™	–	–	SMOS9 LV (18V)*	SMOS8 MV (85V) SMOS8 LV (18V)	SMOS7 MV (45V) SMOS7 LV (18V)	SMOS5 HV+ (105V) HVMOS (30V) SMOS5 LV (18V) SMOS5MV(45V)
RF/IF Silicon	–	–	RF CMOS RF BiCMOS—SiGe (50 GHz) RF BiCMOS—SiGe (120 GHz)	–	RF BiCMOS (24 GHz) RF BiCMOS—SiGe (47 GHz) RF BiCMOS—SiGe (75 GHz)	–
RF/IF III-V	–	–	–	–	–	GaAs pHEMT GaAs Emode2 GaAs HBT (InGaP)

* *Indicates future/limited availability*

CMOS PROCESS TECHNOLOGY

	CMOS 90 nm	CMOS 130 nm	CMOS 0.18 µm	CMOS 0.25 µm	CMOS 0.35 µm
Technology Node	90 nm	130 nm	0.18 µm	0.25 µm	0.35 µm
Wafer Size	200 mm	200 mm	200 mm	200 mm	200 mm
Transistor Nodes	3—low power, general purpose, high performance/SOI	5—low power, general purpose, high performance/SOI (3)	4—general purpose, high performance/SOI (3)	1—general purpose	1—general purpose
Availability	High performance/SOI—Today General purpose—2005	Today	Today	Today	Today
BEOL	Cu (Low K)	Cu (Low K)	Cu	Al	Al
# Metal Layers	5–9	5–9	3–6	3–4	3
# Poly Layers	–	–	1	1–2	1–2
Gate Density	>450K/mm2	>200K/mm2	>100K/mm2	>50K/mm2	>25K/mm2
Foundry Compatible	✓	✓	–	–	–
Static Memory	SRAM, ROM	SRAM, ROM	SRAM, ROM	SRAM, ROM	SRAM, ROM
Nonvolatile Memory	MRAM, eDRAM, Flash, EEPROM (emulated)	Flash, EEPROM (emulated)	–	Flash, EEPROM (emulated)	Flash, EEPROM (true)
Passives	✓	✓	✓	–	–
Libraries	✓	✓	✓	✓	✓
Applications	High-performance logic, mixed-signal, low-power, embedded solutions				

SMARTMOS PROCESS TECHNOLOGY

	SMOS9	SMOS8	SMOS7	SMOS5
Technology Node	0.18 µm	0.25 µm	0.35 µm	>0.40 µm
Wafer Size	200 mm	200 mm	200 mm	150 mm
Voltage Capability	Low voltage (18V)	Low voltage (20V) Mid voltage (80V)	Low voltage (18V) Mid voltage (45V)	Low voltage (18V) Mid voltage (45V) High voltage (105V)
Availability	2005	Today	Today	Today
# Metal Layers	–	3 or 4	3 or 4	2 or 3
# Poly Layers	–	2	2	1 or 2
Gate Density	–	>25K/mm2	>12K/mm2	>5K/mm2
Stand-alone Memory Modules	SRAM	SRAM	SRAM	SRAM
Embedded Memory Modules	ROM	ROM	ROM	ROM
Power Devices	CMOS, LDMOS, bipolar	CMOS, LDMOS, bipolar	CMOS, LDMOS, bipolar	CMOS, LDMOS, bipolar
Analog Devices	–	Low voltage (2.5V, 5.5V, 7.5V, 20V) Mid voltage (2.5V, 5.0V, 10V, 45V, 80V)	Low voltage (3.3V, 7.5V, 10V, 20V, 45V)	–
Libraries	Full mixed-signal/analog design kit	Full mixed-signal/analog design kit	Full mixed-signal/analog design kit	Full mixed-signal/analog design kit
Supports Synthesizable Processor Core	✓	✓	✓	–
Applications	Power management, motor control, high voltage, switching, regulators, mixed signal/analog			

RF/IF SILICON TECHNOLOGY

	180 nm	0.25 µm	0.35 µm
Analog CMOS	✓	✓	✓
RF CMOS	✓	✓	–
BiCMOS	✓	–	✓
BiCMOS-SiGe	✓	–	✓
Analog CMOS			
Technology Node	180 nm	0.25 µm	0.35 µm
Wafer Size	200 mm	–	200 mm
Availability	Today	–	Today
Interconnect	Cu	–	AlCu
Ft	60 GHz	–	–
Devices	MOS: 35A (std Vt and low Vt), 50A or 70A DGO MOS, isolated NMOS, diffused NPN, substrate PNP		MOS: 70A (std Vt, n-ch and p-ch), substrate PNP
Capacitors	Si cap (8 fF/um2, 4.8 fF/um2 or 3.5 fF/um2), MIM cap (1.6 fF/um2 or 5 fF/um2)	–	Double poly cap (1 fF/um2), single poly cap (3.4fF/um2)
Resistors	Si resistor (60 ohm/sq or 375 ohm/sq), poly resistor (1500 ohm/sq), TaN resistor (50 ohm/sq)	–	Si resistors (N-well: 500 ohm/sq or 700 ohm/sq), poly resistor (DPA = 80 ohm/sq), (SPA = 63 ohm/sq)
Applications	Mixed signal, ADC, DAC	–	Mixed signal, ADC, DAC
RF CMOS			
Technology Node	180 nm	0.25 µm	0.35 µm
Wafer Size	200 mm	200 mm	–
Availability	Today	Q4 2004	–
Interconnect	Cu	AlCu	–
Ft	60 GHz	37 GHz	–
Devices	MOS: 35A (std Vt and low Vt), 50A or 70A DGO MOS, isolated NMOS with RFMOS model, diffused NPN, substrate PNP	MOS, isolated NMOS, n+ and p+ VVCs; thick Al inductor	–
Capacitors	Si cap (8 fF/um2, 4.8 fF/um2 or 3.5 fF/um2), MIM cap (1.6 fF/um2 or 5 fF/um2)	MIM, MOS cap with high linearity implant	–
Resistors	Si resistor (60 ohm/sq or 375 ohm/sq), poly resistor (1500 ohm/sq), TaN resistor (50 ohm/sq)	n+ active and poly, p+ poly, high value poly	–
Voltage-Variable Capacitor (VVC) and Inductor	N and P poly VVC single-ended and differential, thick copper inductor (post passivation)	–	–
Applications	Transceiver (LNA, mixer, VCO, synthesizer, TIA)	RF	–

BiCMOS			
Technology Node	180 nm	0.25 µm	0.35 µm
Wafer Size	–	–	200 mm
Availability	–	–	Today
Interconnect	–	–	AlCu
Ft	–	–	24 GHz (npn)
Devices	–	–	MOS: std, low Vt, naturals, isolated NMOS; VVCs and diode varactors; HV CMOS; substrate pnp, thick Al inductor or thick Cu inductor
Capacitors	–	–	MIM, DPC, MIMxDPC
Resistors	–	–	n+ and p+ active and poly, high-value poly, N-well
Applications	–	–	RF
BiCMOS - SiGe			
Technology Node	180 nm	0.25 µm	0.35 µm
Wafer Size	200 mm	–	200 mm
Availability	Today	–	Today
Interconnect	Cu	–	AlCu
Ft	50 GHz, 120 GHz	–	46 GHz, 80 GHz
Devices	SiGe:C HBT NPN. MOS: 35A (std Vt and low Vt), 50A or 70A DGO MOS, isolated NMOS with RFMOS model, diffused NPN, substrate PNP	–	MOS: std, low Vt, naturals, isolated NMOS; VVCs and diode varactors; HV CMOS; substrate pnp, thick Al inductor or thick Cu inductor
Capacitors	Si cap (8 fF/um2, 4.8 fF/um2 or 3.5 fF/um2), MIM cap (1.6 fF/um2 or 5 fF/um2)	–	MIM, DPC, MIMxDPC
Resistors	Si resistor (60 ohm/sq or 375 ohm/sq), poly resistor (1500 ohm/sq), TaN resistor (50 ohm/sq)	–	n+ and p+ active and poly, high-value poly, N-well
Voltage-Variable Capacitor (VVC) and Inductor	N and P poly VVC single-ended and differential, thick copper inductor (post passivation)	–	–
Applications	Transceiver (LNA, mixer, VCO, synthesizer, TIA)	–	RF

RF 7V III-V GaAs TECHNOLOGY

Attribute	Emode 2.5A	InGaP HBT2	PHEMT2	HVPHEMT2	IPD1
Wafer Size	150 mm	150 mm	150 mm	150 mm	150 mm
Gate Length (µ) Emitter Width (µ)	0.85 –	2 –	– 0.6	0.6 –	– –
Vth (V)	0.6	–	-1.2	-1	–
fT (GHz)	19 (20% Imax)	48	23 (Vg=-0.8)	11 (Vg=-0.6)	–
fmax (GHz)	29 (20% Imax)	50–60	–	21 (Vg=-0.6)	–
Operating Voltage (V)	3.2	3.2	3.5	12	–
Resistor	Thin film and epi	Epi	Thin film and epi	Thin film and epi	Thin film
Capacitor	MIM	MIM	MIM	MIM	MIM
Inductor	Au	Au (air bridge)	Au	Au	Au (air bridge)
Substrate Via	✓	✓	✓	✓	–
Availability	Today	Today	Limited	Limited	Limited
Future Generations	✓	✓	✓	✓	✓

PACKAGING AND TEST TECHNOLOGY

Technology	Description	Highlighted Features/Specifications
Flip-Chip PBGA Assembly	Production-proven, flip-chip PBGA assembly process includes equipment and tooling set, materials list, process recipes and specifications, control plans and FMEAs, packaging design guidelines, development and production process, and knowledge transfer.	Packaging Capability: package size up to 50 mm x 50 mm, BGA ball count 1200+, BGA pitch 0.8 mm to 1.27 mm, die size up to 15 mm x 15 mm, bump count 1700+, bump pitch 200 µm, bump composition Pb97Sn03, Pb95Sn05, Pb37Sn63. Manufacturing Capability: pick and place directly from wafers to substrate, speed sort at die attach, capacitor attach, laser mark on back of die, package lid, no-clean die attach flux.
Electroplated Bumping Technology	Production-proven electroplate wafer-bumping process includes equipment and tooling set, process recipes, materials list, bump-design guidelines, development and production process knowledge transfer, Freescale documentation, training and support.	Bump dia/pitch: 100 µm/150 µm; bond pads: aluminum and pure Cu; bump alloy: high Pb (Pb95Sn05)/eutectic (Pb37Sn63)/low alpha Pb/Pb-free; wafer diameters: 100 mm to 200 mm Enables other applications: integrated passives, wafer-level CSP, sacrificial metal wafer-level burn-in and test process.
Wafer-Level Burn-In and Test: Sacrificial Metal Method	Production-proven WLBT: sacrificial metal technology enables known good die and lowers total product cost through increased yields and simplified process flow. Technology includes sacrificial metal circuit design methodology, process technology and equipment and fixture design and sources.	5-inch and 8-inch processes qualified. Technology transfer includes complete technology documentation and patent coverage, training and support through qualification, access to valuable patents.
Wafer-Level Burn-In: Direct Contact Method	Burn-in and test methodology for die at the wafer level provides massive parallel test capabilities and lowers total product cost through elimination of package-level burn-in and reduction of test time at probe and final test, increased test yields and simplified process flow; utilizes a direct contact per die method; provides a robust, full-wafer contact process; and enables known good die (KGD), SiP and MCM technologies. Technology includes process technology, equipment and fixture design and sources, documentation, training and support.	Multiuse contactors. Available for wafers up to 300 mm in diameter.
Power QFN Package	A Freescale innovation, the Power QFN (PQFN) is a single or multi-chip option to the HSOP package. The PQFN is available in both standard and custom configurations. Technology includes patents, design and process know-how.	The PQFN offers superior thermal performance and proven solder joint reliability. The small footprint is JEDEC approved. The PQFN is a cost-effective packaging alternative for multi-chip applications.
Array QFN Package	The Array QFN developed by Freescale is a lead-frame-based, chip-scale semiconductor package offering low-cost, high-thermal performance and high I/O density. The package is a multi-row version of the standard Quad Flat Pack No-Lead (QFN) package. Technology includes patents, design and process know-how.	The Array QFN bridges the gap between standard QFN and MAP BGA packages by offering a low-cost alternative for 80 to 120 I/O devices. The I/O density, combined with excellent thermal dissipation capability, makes the Array QFN an attractive package.
QuickTest™ Test Time Reduction	Statistical software solution employs a unique, patented methodology to reduce test time 5 percent to 25 percent while maintaining a six-sigma level of quality.	Three-part architecture includes automated analysis; Web-based, real-time reporting accessible anywhere in the world; and data storage. More than 30 million devices have been QuickTested with zero product returns. Used on digital and mixed-signal semiconductor products at both probe and final test.

MATERIALS AND EQUIPMENT TECHNOLOGY

Technology		Description	Highlighted Features/Specifications	Product Applications
Modeling Software Databases—Plasma Chemistries	Research IP	Software databases that model the chemical species formation and interaction in plasma environments; currently focused on etch chemistries, such as CxFx.	Detailed chemical species modeling throughout a plasma process.	Plasma process development, plasma processing equipment development.
Modeling Software—Photolithography	Research IP	Software program to model photolithographic effects of multiple layer film stacks, photo dose, layout shapes, reticle enhancement technologies, etc.	Program handles both standard and EUV modeling; provides rapid 2D modeling capability.	Photolithography research, bitcell design.
Equipment Improvements—CMP	Manufacturing IP	Equipment modifications for chemical mechanical polishing (CMP) that increase equipment reliability and reduce complexity and process scrap.	Patent-pending improvements to mass-market equipment.	Semiconductor manufacturing, compact disc or other polishing applications.
Copper Slurry Chemistries	Manufacturing IP	Proprietary slurry chemistries developed for copper polishing.	Proven on high-yielding 0.13 µm CMOS process.	Semiconductor manufacturing, other copper polishing applications.
Equipment Improvements—Metal Sputter	Manufacturing IP	Equipment modifications for metal sputtering.	Provides improved control over sputtering process, as well as increased sputtering kit life.	Semiconductor manufacturing, equipment development.
Plating Chemistries and Processes	Manufacturing IP	Proprietary chemistries developed for specialized metal-plating requirements.	Ultrapure coatings with excellent controllability of layer thickness.	Semiconductor manufacturing, ultrathin metallic plating.

DESIGN IP

Technology
Microprocessors and Microcontrollers
Embedded Memories
Data Converters
Frequency Generation
Peripherals
Power Amplifiers
Power Management
Receivers
Signal Processing
Transmitters

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