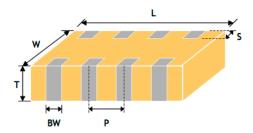
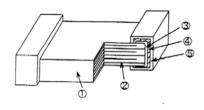
Multilayer Ceramic Capacitor Array - GMY Series





■Construction and Dimensions





Scope

- Cal-Chip's capacitor arrays are developed to offer designers the opportunity to lower placement costs and increase assembly line output through lower component count per board.

No.	Naı	me	NP0, X7R, Y5V
0	Ceramic	material	BaTiO₃ based
2	Inner el	ectrode	Ni
3		Inner layer	Cu
4	Termination	Middle layer	Ni
(5)		Outer layer	Sn (Matte)

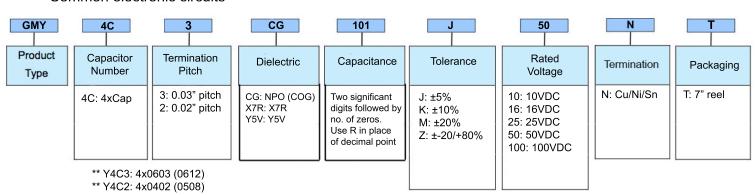
■ Features

- High density mounting due to mounting space saving.
- Mounting cost saving
- Increased throughput
- RoHS compliant
- HALOGEM compliant

Size Inch(mm)	L (mm)	W (mm)	T (mm)	S (mm)	BW (mm)	P (mm)
4x0402 0508 (1220)	2.00±0.15	1.25±0.15	0.85±0.10	0.20±0.10	0.25±0.10	0.50±0.10
4x0603 0612 (1632)	3.20±0.15	1.60±0.15	0.80±0.10	0.30±0.20	0.40±0.15	0.80±0.15

Applications

- Use as a bypass for digital and analog signal line noise
- Computer motherboards and peripherals
- Common electronic circuits





■ Capacitance Range

DIMENS	ION (MM)			G	MY4	C2						GM	Y4C3			
L((L1)	1		2	.00±0.1	.5			3.20±0.15							
1	w	1		1	.25±0.1	.5						1.60:	±0.15			
Diel	ectric		COG			X	7R			COG			X7R		Y!	5V
Н (max)	 	0.95			0.	95			0.90			0.9	-	_	90
-	Voltage	25	50	100	10	16	25	50	25	50	100	16	25	50	16	50
	Range	- 23	30	100	10	10	2.5	30	23	50	100	10	23	30	10	- 50
	100						_						_			⊢
10pF 15	150											_	_			-
22	220															
33.0	330															$\overline{}$
47	470	N 27		1												
68	680															
100	101		:		1									ŗ.,		
150	151	- 1														
180	181															
220	221				,						,-			,		
270	271	(4			122						, i			5× 5+		
330	331															
470	471															
680	681				,											
1000	102													-		
1500	152		1		.*		,				1					
2200	222															
3300	332			1										,		
4700	472												12			
6800	682			-	7								P			
0.010uF	103										,					
0.015	153			1										e,		
0.022	223															
0.033	333						l i									
0.047	473															
0.068	683								1		-					
0.10	104										7					

■ General Electrical Data

Dielectric	N	P0	X7	'R	Y5V
Size	4x0402	4x0603	4x0402	4x0603	4x0603
Inch (mm)	0508 (1220)	0612 (1632)	0508 (1220)	0612 (1632)	0612 (1632)
Capacitance*	10pF to 270pF	10pF to 470pF	1000pF to 100nF	180pF to 100nF	10nF to 100nF
Capacitance tolerance**	J (±5%), K (±10%)		K (±10%),	Z (-20/+80%)	
Rated voltage (WVDC)	25, 50\	/, 100V	10V, 16V, 25V, 50V	16V, 25V, 50V	16V, 50V
Q/Tan δ*	Cap<30pF: Q≥400+20C Cap≥30pF: Q≥1000		Ur=50V, ≤2.5% Ur=25V&16V, ≤3.5% Ur=10V, ≤5.0%		Ur=50V, ≤5% Ur=16V, ≤7%
Insulation resistance at Ur	≥10GΩ		≥10GΩ (chever is less	
Operating temperature	-55 to		+125°C	-25 to +85°C	
Capacitance characteristic	±30ppm		±15	+30/-80%	
Termination			Ni/Sn (lead-free termination)		

^{*} Measured at 30~70% related humidity.

NP0: Apply 1.0±0.2Vrms, 1.0MHz±10% at the conditions of 25°C ambient temperature.

X7R: Apply 1.0 \pm 0.2Vrms, 1.0kHz \pm 10%, at the conditions of 25°C ambient temperature.

Y5V: Apply 1.0±0.2Vrms, 1.0kHz±10%, at the conditions of 20°C ambient temperature.

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^{**} Preconditioning for Class II MLCC: Perform a heat treatment at 150±10°C for 1 hour, then leave in ambient condition for 24±2 hours before measurement.



■ Reliability Test Conditions and Dimensions

No.	Item		Test Condition			Requirements		
1.	Visual and				* No remark	able defect.		
	Mechanical				* Dimensions to conform to individual specification sheet.			
2.	Capacitance	Class I: (NP0))		* Shall not exceed the limits given in the detailed spec.			
3.	Q/ D.F.	1.0±0.2Vrms	1.0±0.2Vrms, 1MHz±10%			≥30pF, Q≥1000; Cap<30pF, Q≥400+	20C	
	(Dissipation	Class II: (X7F	Class II: (X7R, Y5V)			50V, ≤2.5%; Ur=25V&16V, ≤3.5%; Ur	=10V, ≤5.0%	
	Factor)	1.0±0.2Vrms,	, 1kHz±10%		Y5V: Ur=	50V, ≤5%; Ur=16V, ≤7%		
4.	Dielectric	* To apply 25	0% rated voltage.		* No eviden	ce of damage or flash over during tes	st.	
	Strength	* Duration: 1 to 5 sec.						
		* Charge and	discharge current less than 50m.	A.				
5.	Insulation	To apply rate	d voltage for max. 120 sec.		≥10GΩ or R	xC≥500Ω-F whichever is smaller.		
	Resistance							
6.	Temperature	With no elect	rical load.					
	Coefficient	T.C.	Operating Temp	1	T.C.	Capacitance Change		
		NP0	-55~125°C at 25°C		NP0	Within ±30ppm/°C		
		X7R	-55~125°C at 25°C	-	X7R	Within ±15%		
		Y5V	-25~85°C at 20°C]	Y5V	Within +30%/-80%		
7.	Adhesive	* Pressurizing	g force :		* No remarkable damage or removal of the terminations.			
	Strength of	5N (≤0603)) and 10N (>0603)					
	Termination	* Test time: 1	0±1 sec.					
8.	Vibration	* Vibration fre	equency: 10~55 Hz/min.		* No remark	cable damage.		
	Resistance	* Total amplit	ude: 1.5mm		* Cap change and Q/D.F.: To meet initial spec.			
		* Test time: 6	hrs. (Two hrs each in three mutu	ally				
		perpendicula	r directions.)					
		* Measureme	ent to be made after keeping at ro	om temp. for				
		24±2 hrs.						
9.	Solderability	* Solder tem	perature: 235±5°C		95% min. co	overage of all metalized area.		
		* Dipping tim	e: 2±0.5 sec.					
10.	Bending Test	* The middle	part of substrate shall be pressur	rized by means	* No remarkable damage.			
		of the pressu	rizing rod at a rate of about 1 mm	per second until	* Cap change :			
		the deflection	n becomes 1 mm and then the pre	essure shall be	NP0: within ±5.0% or ±0.5pF whichever is larger.			
		maintained fo	or 5±1 sec.		X7R: within ±12.5%			
		* Measureme	ent to be made after keeping at ro	om temp. for	Y5V: within ±30%			
		24±2 hrs.			(This capac	itance change means the change of	capacitance under	
				specified flexure of substrate from the capacitance measured befo				
					the test.)			
11.	Resistance to	* Solder tem	perature: 260±5°C		* No remark	cable damage.		
	Soldering Heat	* Dipping tim	e: 10±1 sec		* Cap chang	ge:		
	* Preheating: 120 to 150°C for 1 minute before immerse the capacitor in a eutectic solder.		NP0: within ±2.5% or ±0.25pF whichever is larger.					
			X7R: within ±7.5%					
		* Before initia	al measurement (Class II only): Pe	erform	Y5V: within ±20%			
	!	150+0/-10°C	for 1 hr and then set for 24±2 hrs	at room temp.	* Q/D.F., I.R	and dielectric strength: To meet init	ial requirements.	
		* Measureme	ent to be made after keeping at ro	om temp. for	* 25% max.	leaching on each edge.		
		24±2 hrs.	× 6.4					

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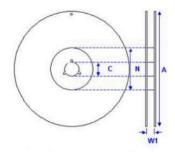
No.	Item		Test Condition		Requirements	
12.	Temperature Cycle	* Conduct	the five cycles according to the tem	peratures and	* No remarkable damage. * Cap change :	
		Step	Temp. (°C)	Time (min.)	NP0: within ±2.5% or ±0.25pF whichever is larger.	
		1		30±3	X7R: within ±7.5%	
		2	Room temp.	2~3	Y5V: within ±20%	
				30±3	* Q/D.F., I.R. and dielectric strength: To meet initial requirements.	
		4	Room temp.	2~3		
		* Before in	nitial measurement (Class II only): P	erform		
		150+0/-10	°C for 1 hr and then set for 24±2 hrs	s at room temp.		
		* Measure	ement to be made after keeping at ro	oom temp. for		
		24±2 hrs.				
13.	Humidity	* Test tem	p.: 40±2°C			
	(Damp Heat)	* Humidity	r: 90~95% RH		* No remarkable damage.	
	Steady State	* Test time	e: 500+24/-0hrs.		* Cap change: NP0: within ±5.0% or ±0.5pF whichever is larger.	
		*Before in	itial measurement (Class II only): Pe	erform	X7R: within ±12.5%	
		150+0/-10°C for 1 hr and then set for 24±2 hrs at room temp.			Y5V: within ±30%	
		* Measurement to be made after keeping at room temp. for			* Q/D.F. value:	
		24±2 hrs			NP0: Cap≥30pF, Q≥350; 10pF≤Cap<30pF, Q≥275+2.5C	
					Cap<10pF; Q≥200+10C	
					X7R: Ur=50V, ≤3%; Ur=25V&16V, ≤5%; Ur=10V, ≤7.5%	
					Y5V: Ur=50V, ≤7.5%; Ur=16V, ≤10%	
					* l.R.: ≥1GΩ or RxC≥50Ω-F whichever is smaller.	
14.	Humidity	* Test tem	p.: 40±2°C		* No remarkable damage.	
	(Damp Heat)	* Humidity	r: 90~95%RH		* Cap change: NP0: within ±7.5% or ±0.75pF whichever is larger.	
	Load	* Test time	e: 500+24/-0 hrs.		X7R: within ±12.5%	
		* To apply	voltage: rated voltage.		Y5V: within ±30%	
		* Before in	nitial measurement (Class II only): To	o apply test	* Q/D.F. value:	
		voltage for	r 1hr at 40°C and then set for 24±2 h	nrs at room temp.	NP0: Cap≥30pF, Q≥200; Cap<30pF, Q≥100+10/3C	
		* Measure	ement to be made after keeping at ro	oom temp. for	X7R: Ur=50V, ≤3%; Ur=25V&16V, ≤5%; Ur=10V, ≤7.5%	
		24±2 hrs	•		Y5V: Ur=50V, ≤7.5%; Ur=16V, ≤10%	
					* I.R.: ≥500MΩ or RxC≥25Ω-F whichever is smaller.	
15.	High	* Test tem	p.:		* No remarkable damage.	
	Temperature	NP0, X7	R: 125±3°C		* Cap change: NP0: within ±3.0% or ±0.3pF whichever is larger.	
	Load	Y5V: 85:	±3°C		X7R: within ±12.5%	
	(Endurance)	* To apply	voltage: 200% of rated voltage.		Y5V: within ±30%	
			e: 1000+24/-0 hrs.		* Q/D.F. value:	
		*Before in	itial measurement (Class II only): To	apply test	NP0: Cap≥30pF, Q≥350	
			r 1hr at test temp. and then set for 2		10pF≤Cap<30pF, Q≥275+2.5C	
		temp.	30 \$1		Cap<10pF, Q≥200+10C	
			ment to be made after keeping at ro	om temp. for	X7R: Ur=50V, ≤3%; Ur=25V&16V, ≤5%; Ur=10V, ≤7.5%	
		24±2 hrs	and the same and analysis of the same of the same of		Y5V: Ur=50V, ≤7.5%; Ur=16V, ≤10%	
					* I.R.: ≥1GΩ or RxC≥50Ω-F whichever is smaller.	

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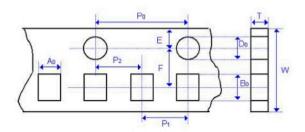
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■ Packaging



Paper Tape Specifications



Size	Thickness	Paper Tape
4x0402 0508 (1220)	0.85±0.10	4K
4x0603 0612 (1632)	0.80±0.10	4K

SIZE Inch (mm)	4x0402 0508 (1220)	4x0603 0612 (1632)
Thickness	T	В
Ao	1.50±0.10	2.00±0.10
Bo	2.30±0.10	3.50±0.10
Т	0.95±0.05	0.95±0.05
K ₀		-
w	8.00±0.10	8.00±0.10
Po	4.00±0.10	4.00±0.10
10xP₀	40.0±0.10	40.0±0.10
P ₁	4.00±0.10	4.00±0.10
P ₂	2.00±0.05	2.00±0.05
D ₀	1.55±0.05	1.50±0.05
D ₁	-	-
E	1.75±0.05	1.75±0.10
F	3.50±0.05	3.50±0.05

Reel size	7"		
С	13.0+0.5/-0.2		
W ₁	8.4+1.5/-0		
A	178.0±0.10		
N	60.0+1/-0		

Storage and Handling Conditions

- (1) To store products at 5 to 40°C ambient temperature and 20 to 70%. related humidity conditions.
- (2) The product is recommended to be used within one year after shipment. Check solderability in case of shelf life extension is needed.

Cautions:

- a. The corrosive gas reacts on the terminal electrodes of capacitors, and results in the poor solderability.
 Do not store the capacitors in the ambience of corrosive gas (e.g., hydrogen sulfide, sulfur dioxide, chlorine, ammonia gas etc.)
- b. In corrosive atmosphere, solderability might be degraded, and silver migration might occur to cause low reliability.
- c. Due to the dewing by rapid humidity change, or the photochemical change of the terminal electrode by direct sunlight, the solderability and electrical performance may deteriorate. Do not store capacitors under direct sunlight or dewing condition. To store products on the shelf and avoid exposure to moisture.

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■ Recommended Solering Conditions

The lead-free termination MLCCs are not only to be used on SMT against lead-free solder paste, but also suitable against lead-containing solder paste. If the optimized solder joint is requested, increasing soldering time, temperature and concentration of N_2 within oven are recommended.

