

Multilayer Ceramic Chip Capacitors



Introduction

Multilayer Surface Mount Ceramic Capacitors are constructed by screen printing alternative layers of internal metallic electrodes onto ceramic dielectric materials and firing into a concrete monolithic body, then completed by application of metal end terminations which are fired to assure permanent bonding with the individual internal electrodes.

Multilayer ceramic capacitors have various features such as large capacitance values in small sizes and excellent high frequency characteristics.

Moreover, chip capacitors can be used on surface mount assembly equipment. Our fully integrated manufacturing and total quality control systems ensure unprecedented high standards of quality and reliability.

Chip Capacitor Selection

Selection of the most suitable capacitor for any application is based on the following:

Dielectric Type

The choice of dielectric is largely determined by the temperature stability required.

COG (NPO)

Capacitance change with temperature is 0-30ppm/°C which is less than -0.3%/°C from -55°C to +125°C. Typical capacitance change with life is less than -0.1% for NPOs, one-fifth that shown by most other dielectrics. NPO formulations show no aging characteristics.

X7R/X5R

Its temperature variation of capacitance is within $\pm 15\%$ from -55°C to +125°C (-55°C to +85°C for X5R). The capacitance change is non-linear.

Z5U

Despite their capacitance instability, Z5U formulations are very popular because of their small size, temperature range low ESL, low ESR and excellent frequency response. These features are particularly important for decoupling application where only a minimum capacitance value is required.

Y5V

Y5V formulations are for general purpose use in a limited temperature range. They have a wide temperature characteristic of +22% - 82% capacitance change over the operating temperature range of -30°C to +85°C. Y5Vs high dielectric constant allows the manufacture of very high capacitance values (up to 22MF) in small physical sizes.

Capacitance Value & Tolerance

Determined by circuit requirements. Note that chip prices decrease with lower capacitance value and looser tolerance.

Voltage

Determined by circuit requirements. Units are designed to exceed the withstanding voltage specification, i.e., the user need not incorporate an additional safety margin.

Capacitor Size

Select the smallest unit permitted by the circuit constraints that provides the required capacitance and voltage rating. All Cal-Chip capacitors conform to EIA specifications.

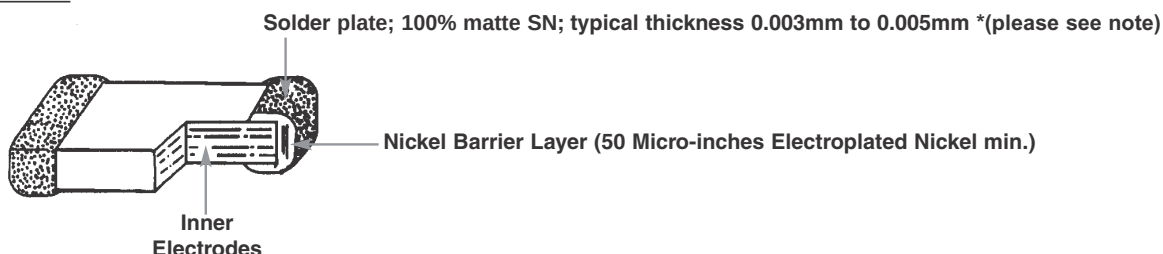
Capacitor Termination

Nickel barrier is standard and recommended for units exposed to repeated solder cycles, to minimize leaching of the termination.

Multilayer Ceramic Chip Capacitors



Construction



Example

GMC21

Size Code

CG

Dielectric

102

Capacitance (pF)

J

Capacitance Tolerance (EIA Code)

50

Voltage

N

Termination

T

Packaging Code

CG (COG) (NPO)
X7R or X5R
Z5U
Y5V

Capacitance values are represented in 3 digits, and expressed in pF. The first two digits are significant, and the third is the number of zeros. The letter "R" is used as a decimal point.

0R5	0.5pF
5R0	5pF
100	10pF
101	100pF
102	1000pF
103	.01uF
104	.1uF
105	1.0uF
106	10uF

B	±0.1pf	for ≤ 10pF
C	±0.25pF	for ≤ 10pF
D	±0.5pF	for ≤ 10pF
F	±1%	
G	±2%	
J	±5%	
K	±10%	
M	±20%	
Z	-20%~+80%	

6r3	6.3 DC
10	10 DC
16	16 DC
25	25 DC
50	50 DC
100	100 DC
200	200 DC

N Nickel Barrier

NX* - Optional "SoftTerm"

Available in select values, contact your sales associate for more information

T* Tape and Reel

*Optional "TD" designates large 10 inch or 13 inch reels - see packaging on pg.13 & 14

GMC02 = 0201	GMC21 = 0805	GMC40 = 1808	GMC55 = 2220
GMC04 = 0402	GMC31 = 1206	GMC43 = 1812	GMC57 = 2225
GMC10 = 0603	GMC32 = 1210	GMC45 = 1825	

Note: Calchip has completed the Lead-Free transition. All parts shipped with or without the "custom designator" LF at the end of the part number will be Lead-Free. Lead-Free material will still continue to have an LF at the end of the Lot Code and a green RoHS symbol on the label. Please contact your sales associate if you require non-RoHS material.

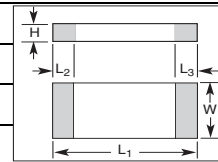


0201

DIMENSION (MM)

GMC02

L(L1)		0.6 ± 0.03					
W		0.3 ± 0.03					
H		0.3 ± 0.03					
BW(L2/L3)		0.15 ± 0.05					
dielectric		NPO/COG	X5R		X7R		Y5V/Z5U
Rated Voltage		25	6.3	10	6.3	10	16
Cap. Range							
0.5pF	0R5						
1.0	1R0						
1.2	1R2						
1.5	1R5						
1.8	1R8						
2.2	2R2						
2.7	2R7						
3.3	3R3						
3.9	3R9						
4.7	4R7						
5.6	5R6						
6.8	6R8						
8.2	8R2						
10	100						
12	120						
15	150						
18	180						
22	220						
27	270						
33	330						
39	390						
47	470						
56	560						
68	680						
82	820						
100	101						
120	121						
150	151						
180	181						
220	221						
270	271						
330	331						
390	391						
470	471						
560	561						
680	681						
820	821						
1.0nF	102						
1.2	122						
1.5	152						
1.8	182						
2.2	222						
2.7	272						
3.3	332						
3.9	392						
4.7	472						
5.6	562						
6.8	682						
8.2	822						
10	103						
12	123						
15	153						
18	183						
22	223						
27	273						
33	333						
39	393						
47	473						
56	563						
68	683						
82	823						
100	104						
120	124						
150	154						
180	184						
220	224						
270	274						
330	334						
390	394						
470	474						
560	564						
680	684						
820	824						
1.0uF	105						
2.2	225						



The diagram shows a rectangular plate with a height H and a width L_1 . The plate is divided into three vertical sections by two vertical lines. The leftmost section has a width L_2 , the middle section has a width L_4 , and the rightmost section has a width L_3 . The total width is $L_1 = L_2 + L_4 + L_3$. The plate is shaded gray.

COG/NPO

A diagram of a rectangular plate with the following dimensions and labels:

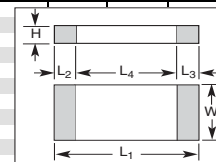
- Height: H
- Width: W
- Length: L_1
- Distance from left edge to first vertical line: L_2
- Distance between the two vertical lines: L_4
- Distance from second vertical line to right edge: L_3



Multilayer Ceramic Chip Capacitors

COG/NPO (cont.)

	GMC21		GMC31		GMC32		GMC40		GMC43		GMC45		GMC55		GMC57	
Type	0805		1206		1210		1808		1812		1825		2220		2225	
Length (L1) mm	2.0±0.3		3.2±0.3		3.2±0.3		4.57±0.25		4.5±0.35		4.5±0.35		5.7±0.4		5.7±0.4	
Inches	0.08±0.012		0.125±0.012		0.125±0.012		0.18±0.01		0.18±0.014		0.18±0.014		0.225±0.016		0.225±0.016	
Width (W) mm	1.25±0.2		1.6±0.2		2.5±0.3		2.03±0.25		3.2±0.3		6.3±0.4		5.0±0.4		6.3±0.4	
Inches	0.05±0.008		0.063±0.008		0.10±0.012		0.08±0.01		0.125±0.012		0.25±0.016		0.197±0.016		0.25±0.016	
Thick(Max) mm	1.3		1.6		1.8		2.03		1.8		1.8		1.8		1.8	
(H) Inches	0.051		0.063		0.07		0.08		0.07		0.07		0.07		0.07	
Termination Band (L2+L3) mm	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Inches	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75
Band Gap mm	0.5		1.4		1.4		2.0		2.2		2.2		2.9		2.9	
(L4) Inches	0.019		0.055		0.055		0.078		0.087		0.087		0.114		0.114	
Rated Voltage d.c.	100	200	100	200	100	200	100	200	100	200	100	200	100	200	100	200
Cap. Range																
Code																
0.5pF	0R5															
1.0	1R0															
1.2	1R2															
1.5	1R5															
1.8	1R8															
2.2	2R2															
2.7	2R7															
3.3	3R3															
3.9	3R9															
4.7	4R7															
5.6	5R6															
6.8	6R8															
8.2	8R2															
10	100															
12	120															
15	150															
18	180															
22	220															
27	270															
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470	474															
560	564															
680	684															
820	824															
1.0nF	105															
2.2	225															
3.3	335															
4.7	475															
6.8	685															
10	106															
22	226															
33	336															
47	476															
68	686															
100	107															



The diagram shows a rectangular plate with a central white area and two gray rectangular regions on the left and right sides. The total width of the plate is labeled L_1 . The width of the central white area is labeled L_4 . The width of each gray region is labeled L_2 (left) and L_3 (right). The height of the plate is labeled H . The width of the plate is also labeled W .

X7R (cont)

		GMC21			GMC31			GMC32			GMC40			GMC43			GMC45			GMC55			GMC57		
Type		0805			1206			1210			1808			1812			1825			2220			2225		
Length(L1)	mm	2.0±0.3			3.2±0.3			3.2±0.3			4.57±0.25			4.5±0.35			4.5±0.35			5.7±0.4			5.7±0.4		
	Inches	0.08±0.012			0.125±0.012			0.125±0.012			0.18±0.01			0.18±0.014			0.18±0.014			0.225±0.016			0.225±0.016		
Width (W)	mm	1.25±0.2			1.6±0.2			2.5±0.3			2.03±0.25			3.2±0.3			6.3±0.4			5.0±0.4			6.3±0.4		
	Inches	0.05±0.008			0.063±0.008			0.10±0.012			0.08±0.01			0.125±0.012			0.25±0.016			0.197±0.016			0.25±0.016		
Thick(Max)	mm	1.3			1.8			2.8			3.0			3.0			3.2			3.5			3.5		
	Inches	0.051			0.063			0.07			0.08			0.07			0.07			0.07			0.07		
Termination Band (L2+L3)	mm	Min	Max		Min	Max		Min	Max		Min	Max		Min	Max		Min	Max		Min	Max		Min	Max	
	Inches	0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75	
Band Gap	mm	0.5			1.4			1.4			2.0			2.2			2.2			2.9			2.9		
	Inches	0.019			0.055			0.055			0.078			0.087			0.087			0.114			0.114		
Rated Voltage d.c.		50	100	200	50	100	200	50	100	200	50	100	200	50	100	200	50	100	200	50	100	200	50	100	200
Cap. Range	Code																								
0.5pF	0R5																								
1.0	1R0																								
1.2	1R2																								
1.5	1R5																								
1.8	1R8																								
2.2	2R2																								
2.7	2R7																								
3.3	3R3																								
3.9	3R9																								
4.7	4R7																								
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2.2	225																								
3.3	335																								
4.7	475																								
6.8	685																								
10	106																								
22	226																								

X5R

The diagram shows a rectangular plate with a total length L_1 and total width H . The plate is divided into three vertical sections. The leftmost section has a width of L_2 , the middle section has a width of L_4 , and the rightmost section has a width of L_3 . The total length is indicated by a dimension line at the bottom labeled L_1 . The total width is indicated by a dimension line on the left labeled H . The width of the middle section is labeled L_4 with arrows pointing to its boundaries. The width of the rightmost section is labeled L_3 with arrows pointing to its boundaries. The width of the leftmost section is labeled L_2 with arrows pointing to its boundaries. The width of the rightmost section is also labeled W with arrows pointing to its boundaries.

Y5V/Z5U

A diagram of a rectangular plate with dimensions L_1 , L_2 , L_3 , L_4 , H , and W . The plate is shown in two views: a top view and a side view. The top view shows a rectangle with width L_1 and height W . The side view shows a rectangle with width L_2 and height H . The distance between the two views is L_4 . The distance from the left edge of the top view to the left edge of the side view is L_3 .

Y5V/Z5U (cont)

[illegible]



COG Dielectric

Ultra stable class I dielectric: linear temperature coefficient, low loss, negligible change of electrical properties with time, voltage and frequency.

Operating Temperature Range	Temperature Coefficient	Temperature Voltage Coefficient (ΔC_{Max} @ V_{DCW})	Dissipation Factor	Insulation Resistance	Dielectric withstanding Voltage	Aging Rate	Test Parameters
-55°C to +125°C	0±30ppm/°C	0±30ppm/°C	0.1% Max, 0.02% Typical	• 25°C, V_{DCW}: >100GΩF or 1000ΩF, whichever is less • 125°C, V_{DCW}: >10GΩF or 100ΩF, whichever is less	3 X V_{DCW}	0% per decade hour	• $C \leq 1000pF$ f=1MHz V=1.0Vrms ±0.2Vrms T=25°C • $C > 1000pF$ f=1KHz V=1.0Vrms ±0.2Vrms T=25°C

X7R/X5R Dielectric

Stable class II dielectric

Operating Temperature Range	Temperature Coefficient	Temperature Voltage Coefficient (ΔC_{Max} @ V_{DCW})	Dissipation Factor	Insulation Resistance	Dielectric withstanding Voltage	Aging Rate	Test Parameters
X7R = -55C to +125C X5R = -55C to +85C	±15%	X7R/X5R Not Applicable	2.5% Max, 1.8% Typical	• 25°C, V_{DCW}: >100GΩFor 1000ΩF, whichever is less • 125°C, V_{DCW}: >10GΩF or 100ΩF, whichever is less	2.5 X V_{DCW}	<2% per decade hour	1KHz, 1.0Vrms ±0.2Vrms 25°C values > or = to 10uF 1.0Vrms 120Hz

Multilayer Ceramic Chip Capacitors - Z5U (Y5V) Dielectric

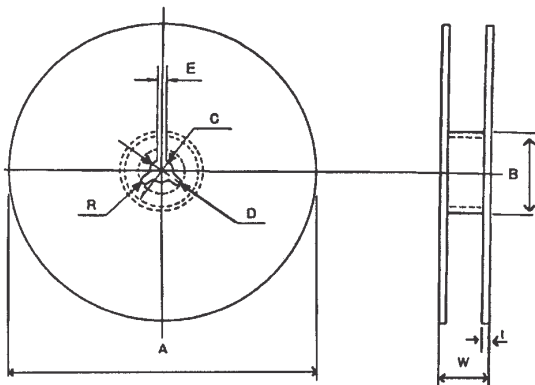


High capacitance per unit volume: general purpose product

Operating Temperature Range	Temperature Coefficient	Dissipation Factor	Insulation Resistance	Dielectric withstanding Voltage	Aging Rate	Test Parameters
-30°C to +85°C	+22% -82%	3.0% Max, 2.0% Typical	10GΩ or 100ΩF whichever is less, 25°C, VDCW	2.5 X VDCW	3.0% per decade hour	1KHz, 1Vrms 25°C values > or = to 10uF 1.0Vrms 120Hz

Packaging (Taping)

(Reel Type-Size)



Standard Reel

Unit:mm

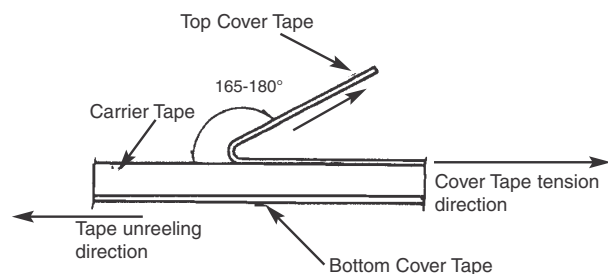
A	B	C	D	E	W	t	R
ø178 ±2.0	ø50 min.	ø13.0 ±0.5	ø21.0 ±0.8	2.0 ±0.5	14.9 ±1.5	0.8 ±0.2	1.0

"TD" designator for optional 10/13 inch reels

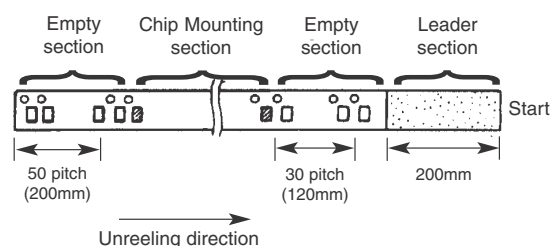
Unit:mm

A	B	C	D	E	W	t	R
ø250 ±2.0	ø50 min.	ø13.0 ±0.5	ø21.0 ±0.8	2.0 ±0.5	10.0 ±1.5	0.8 ±0.2	1.0

Carrier Tape (Standard)



- To peel off the cover tape by the method shown in the right figure apply a peel-off force of 20 gf - 60 gf (card board); 35 gf - 75 gf (plastic tape).
- The cover tape should not touch the top or bottom of the chip.
- If the cover tape has been peeled off it may be difficult to remove the chip due to punch-hole clearance, dirt, and debris. Make sure therefore that no paper waste will adhere to and block the absorption nozzle.
- If the cover tape has been peeled off from the top, stick it back on with a suitable adhesive.
- Follow the illustration for the start and end of the winding operation.



Multilayer Ceramic Chip Capacitors

- Cardboard carrier tape for 0402,0603 type and 0805/1206 type

Unit: mm

Type	A	B	W	F	E	P ₁	P ₂	P ₀	D ₀	t ₁	t ₂	Mounting Hole	Std Reel Qty. 7in (10/13in)*
0402	0.7±0.2	1.3±0.2	8.0±0.3	3.5±0.05	1.75±0.1	4.0±0.1	2.0±0.05	4.0±0.1	ø1.5±0.1	1.1 max	1.4 max	Angular Punch Hole	10,000 (20,000)
0603	1.1±0.2	1.9±0.2											4,000 (10,000)
0805	1.65±0.2	2.4±0.2											4,000 (10,000)
1206	2.0±0.2	3.6±0.2											4,000 (10,000)

*quantities listed are considered as "standard" and subject to change

- Embossed plastic carrier tape for 0805/1206 type and 1210 type

Unit: mm

Type	A	B	W	F	E	P ₁	P ₂	P ₀	D ₀	t ₁	t ₂	Mounting Hole	Std Reel Qty. 7in (10/13in)*
0805	1.45±0.2	2.3±0.2	8.0±0.3	3.5±0.05	1.75±0.1	4.0±0.1	2.0±0.05	4.0±0.1	ø1.5±0.1 -0	0.6 max	2.5 max	Angular Embossed Hole	3,000 (10,000)
1206	2.0±0.2	3.6±0.2											2,500 (10,000)
1210	2.9±0.2	3.6±0.2											2,000 (4,000)

*quantities listed are considered as "standard" and subject to change

- Embossed plastic carrier tape for 1812,1825,2220 and 2225 type

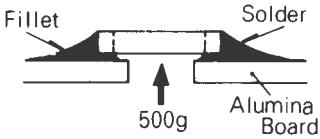
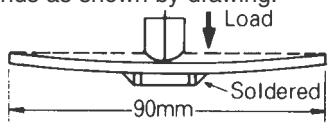
Unit: mm

Type	A	B	W	F	E	P ₁	P ₂	P ₀	D ₀	t ₁	t ₂	Mounting Hole	Std Reel Qty. 7in (10/13in)*
1812	3.6±0.2	4.9±0.2	12.0±0.3	5.5±0.05	1.75±0.1	8.0±0.1	2.0±0.05	4.0±0.1	ø1.5±0.1	0.6 max.	6.5 max.	Angular Embossed Hole	1,000 (2,000)
1825	6.8±0.3	4.9±0.2											1,000 (1,500)
2220	5.5±0.3	6.2±0.3											1,000 (1,500)
2225	6.8±0.3	6.2±0.3											500 (1,000)

*quantities listed are considered as "standard" and subject to change



RELIABILITY AND TEST CONDITIONS

Item	Specification	Test Method
Capacitance	Within tolerance shown by part number code	- Class (I) C<1000pF:1MHz±10%, 0.5 to 5Vrms C≥1000pF:1KHz±10%, 1.0±0.2Vrms - Class (II) 1KHz±10%, 1.0±0.2Vrms values > or = to 10uF 1.0Vrms 120Hz
Dissipation Factor (tanδ or Q)	- Class (I) C<30pF:Q≥400+20xC C≥30pF:Q≥1000 - Class (II) X7R/X5R:DF≤2.5% Y5V/Z5U:DF≤3.0%	
Insulation Resistance(IR)	NPO thru X5R: C≤50,000pF: IR≥100GΩ C>50,000pF: IR≥500MΩ. Per Uf. Y5V/Z5U: IR≥10GΩ	Apply rated voltage for 60 seconds at room temperature and normal humidity. (70% RH max)
Dielectric Withstanding Voltage	There shall be no evidence of damage or flash over during the test	Apply 3 x rated voltage (Class I) or 2.5 x rated voltage (Class II) to both terminations for 5 seconds. Charge and discharge current are less than 50mA.
Termination Adherence	No mechanical damage	 Care shall be taken to avoid thermal shock. 500g of steady pull is applied in direction of arrow for 1 minute.
Bend Strength	No mechanical damage	After soldering capacitor on the glass-epoxy PWB, 2 mm of vending shall be applied for 10 seconds as shown by drawing. 
Life Test (High Temperature Loading Test)	ΔC	Applied 2 x rated voltage at maximum operating temperature for 1000 hours. The surge current shall not exceed 50mA after above testing condition, test samples shall be kept in room temperature for 24 hours (Class I) or 48 hours (Class II), and then shall be measured.
	Q or DF	
	IR	



RELIABILITY AND TEST CONDITIONS

Item	Specification	Test Method
Moisture Test	ΔC - Class (I) No more than $\pm 5\%$ or $\pm 0.5\text{pF}$ whichever is larger - Class (II) X7R/X5R: $\pm 10\%$ Y5V/Z5U: $\pm 30\%$	The capacitors shall be subjected to 40°C, 90-95%RH for 500 hours. After above testing condition, samples shall be kept in room temperature for 24 hours (Class I) or 48 hours (Class II), and then shall be measured.
	Q or DF - Class (I) $C < 10\text{pF}$: $Q > 200 + 10 \times C$ $10 \leq C < 30\text{pF}$: $Q \geq 275 + 5/2 \times C$ $C \geq 30\text{pF}$: $Q \geq 350$ - Class (II) X7R/X5R: $DF \leq 5.0\%$ Y5V/Z5U: $DF \leq 7.5\%$	
	IR 1000M Ω or 50 ΩF , whichever is less	
Moisture Resistance Test	ΔC - Class (I) No more than $\pm 7.5\%$ or $\pm 0.75\text{pF}$ whichever is larger - Class (II) X7R/X5R: $\pm 10\%$ Y5V/Z5U: $\pm 30\%$	Apply rated voltage at 40°C, 90-95%RH for 500 hours. The surge current shall not exceed 50mA. After testing with above condition, samples shall be kept in room temperature for 24 hours (Class I) or 48 hours (Class II), and then shall be measured.
	Q or DF - Class (I) $C < 30\text{pF}$: $Q > 100 + 100/3 \times C$ $C \geq 30\text{pF}$: $Q \geq 200$ - Class (II) X7R/X5R: $DF \leq 5.0\%$ Y5V/Z5U: $DF \leq 7.5\%$	
	IR 500M Ω or 25 ΩF , min whichever is less	
Temperature Cycle	ΔC - Class (I) No more than $\pm 2.5\%$ or $\pm 0.25\text{pF}$ whichever is larger - Class (II) X7R/X5R: $\pm 5\%$ Y5V/Z5U: $\pm 20\%$	Perform 5 cycles as follow: - Room temperature. Dwell for 15 minutes. - Minimum operating temperature, dwell for 30 minutes. - Room temperature, dwell for 30 minutes. - Maximum operating temperature, dwell for 30 minutes. After above testing condition, samples shall be kept in room temperature for 24 hours (Class I) or 48 hours (Class II), and then shall be measured.
	Q or DF To satisfy the specified initial value.	
	IR To satisfy the specified initial value.	
Solderability	Termination area shall be at least 95% covered with a new solder coating. There shall be no crack and ceramic exposure of terminated surface by melting.	The capacitors are completely immersed during 4 ± 0.5 seconds in the molten solder with a temperature of $230 \pm 5^\circ\text{C}$ *Solder: Sn 63.
Resistance to Solder Heat Test	ΔC - Class (I) No more than $\pm 2.5\%$ or $\pm 0.25\text{pF}$ whichever is larger - Class (II) X7R/X5R: $\pm 5\%$ Y5V/Z5U: $\pm 20\%$	Immerse into molten solder at $270 \pm 5^\circ\text{C}$ for 3 ± 0.5 seconds. Preheat before immersion. $80 \sim 100^\circ\text{C}$ for 2 minutes. $150 \sim 180^\circ\text{C}$ for 2 minutes. $270 \pm 5^\circ\text{C}$ for 3 ± 0.5 seconds. The capacitance measurement shall be made after sample keeping at room temperature for 24 hours.
	Q or DF To satisfy the specified initial value.	
	IR To satisfy the specified initial value.	



APPLICATION MANUAL FOR
SURFACE MOUNTING

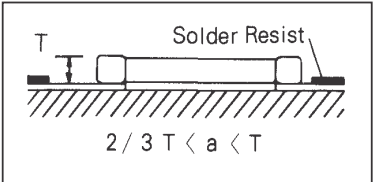
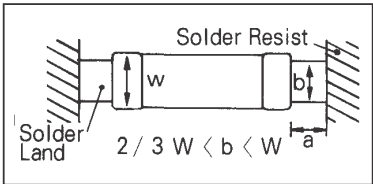
1. Temperature / Humidity Control

Since dew condensation may occur by the differences in temperature when the products are take out of storage, it is important to maintain a temperature-controlled environment.

2. Design of Solder Land Pattern

When designing printed circuit boards, the shape and size of the solder lands must allow for the proper amount of solder on the capacitor. The amount of solder at the end terminations has a direct effect on the probability that the chip will crack. The greater amount of solder, the larger amount of stress on the chip, and the more likely that it will break. Use the following illustrations as guidelines for proper solder land design.

Recommendation of solder land shape and size.



3. Adhesives

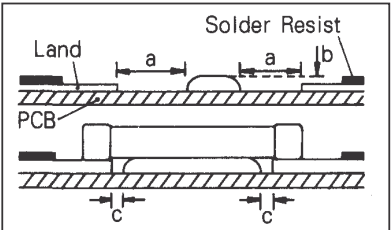
MLCCs generally require the use of an adhesive to adhere the chips to the circuit board prior to wave soldering.

3-1. Requirements for Adhesives

- They must have enough adhesion so that the chips will not fall off or move during the handling of the circuit board.
- They must maintain their adhesive strength when exposed to soldering temperatures.
- They should not spread or run when applied to the circuit board.
- They should have a long pot life.
- They should harden quickly.
- They should not corrode the circuit board or chip material.
- They should be a good insulator.
- They should be non-toxic, and not produce harmful gases, nor be harmful when touched.

3-2. Application Method

It is important to use the proper amount of adhesive. Too little will cause poor adhesion to the circuit board, and too much may strain the conductor pattern, thereby causing defective soldering. The following illustrations show the proper quantity of adhesive.



(Unit: mm)

Type	21	31
a	0.2 min	0.2 min
b	70~100μm	70~100μm
c	>0	>0

3-3. Adhesive Hardening Characteristics

To prevent oxidation of the terminations, the adhesive must harden at 160°C or less, within 2 minutes or less.



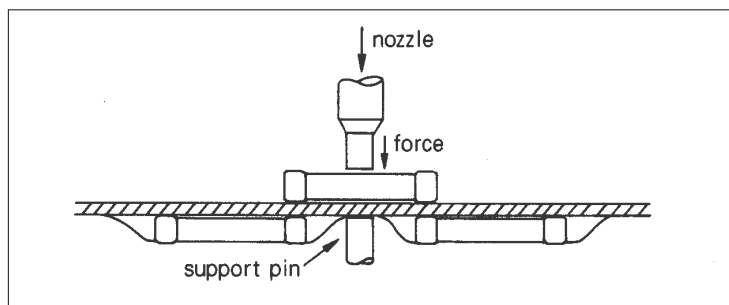
4. Mounting

4-1. Mounting Head Pressure

Excessive pressure will cause chip capacitors to crack. The pressure between nozzle and chip capacitor will be 300g maximum during mounting.

4-2. Bending Stress

Bending of printed circuit board by mounting head when double-sided circuit boards are used, chip capacitors first are mounted and soldered onto one side of the board. When the capacitors are mounted onto the other side, it is important to support the board as shown in the illustration. If the circuit board is not supported, it may bend, causing the already installed capacitors to crack.



5. Flux

Although highly activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, it is recommended that a mildly activated rosin flux (less than 0.2% chlorine) be used.

6. Soldering

Since a multilayer chip ceramic capacitor comes into direct contact with melted solder during soldering, it is exposed to potentially damaging mechanical stress caused by the sudden temperature change. The capacitor may also be subject to silver migration, and to contamination by the flux. Because of these factors, soldering technique is critical.

6-1. Soldering Methods

Method	Classification	
Reflow Soldering	Mass reflow	• IR/Convection • VPS (Vapor phase)
	Selective reflow	• Hot air/gas • Laser
Flow Soldering	Dual Wave	

6-2. Soldering Profile

To avoid the crack problem by sudden temperature change, follow the temperature profile in graph 6-4.



Soldering (Continued)

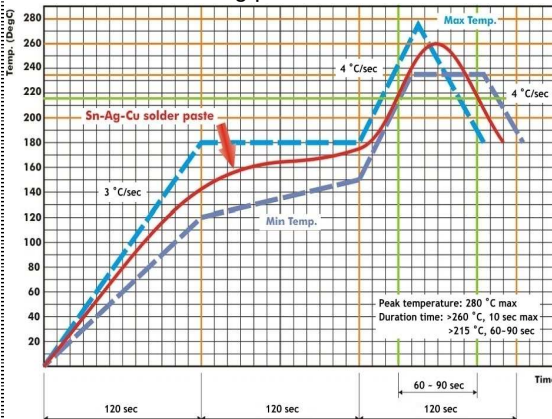
6-3 Flux selection

Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, the following is recommended.

- 1) It is recommended to use a mildly activated rosin flux (less than 0.1 wt% chlorine). Strong flux is not recommended.
- 2) Excessive flux must be avoided. Please provide proper amount of flux.
- 3) When water-soluble flux is used, enough washing is necessary.

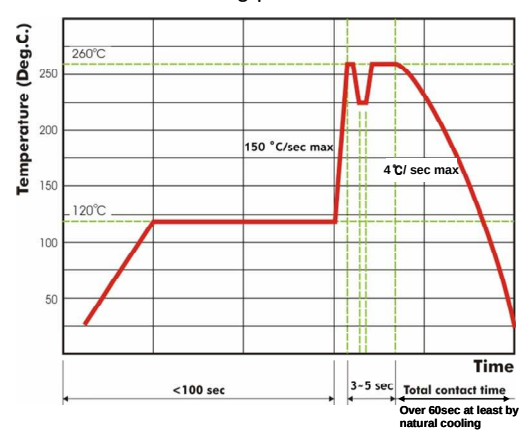
6-4 Recommended soldering profile by various methods

IR reflow soldering profile



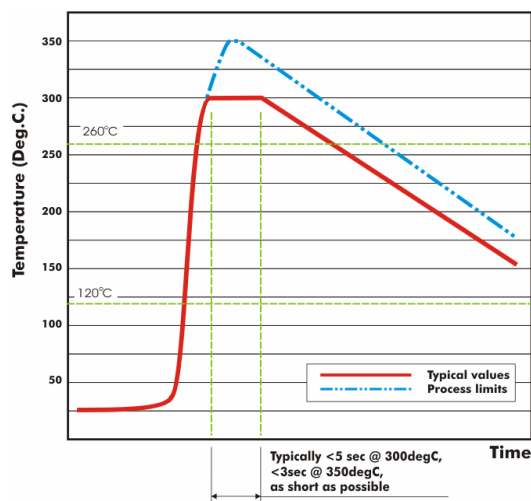
Recommended IR reflow soldering profile for SMT process with SnAgCu series solder paste.

Wave soldering profile



Recommended wave soldering profile for SMT process with SnAgCu series solder.

Manual soldering (solder iron)



Wave soldering is recommended only for the following case sizes:
0603(1608); 0805(2012)&1206(3216)
thickness< 1mm



Soldering (Continued)

6-5 Avoiding thermal shock

1) Preheating condition

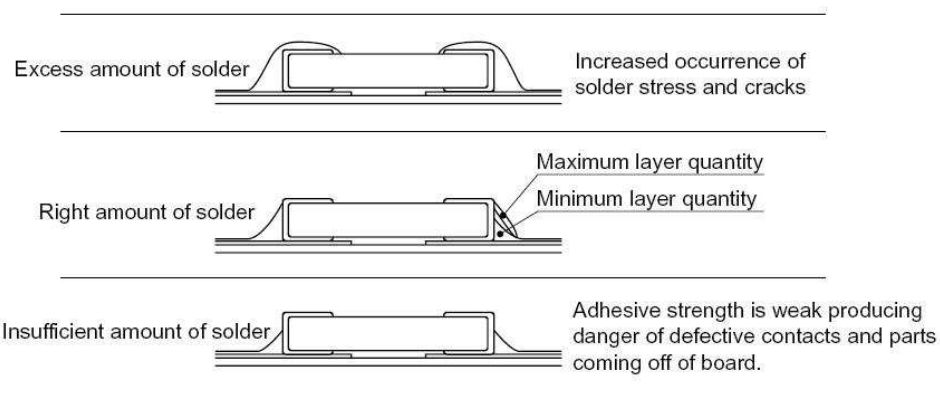
Soldering	Size	Temperature difference(ΔT)
Wave soldering	1206 (3216) or less	$\Delta T \leq 150^{\circ}\text{C}$
Reflow soldering	1206 (3216) or less	$\Delta T \leq 190^{\circ}\text{C}$
	1210 (3225) or more	$\Delta T \leq 130^{\circ}\text{C}$
Manual soldering	1206 (3216) or less	$\Delta T \leq 190^{\circ}\text{C}$
	1210 (3225) or more	$\Delta T \leq 130^{\circ}\text{C}$

2) Cooling condition

Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) must be less than 100°C .

6-6 Amount of solder

Excessive solder will induce higher tensile force in chip capacitor when temperature changes and may result in chip cracking. Insufficient solder may detach the capacitor from the P.C. board.



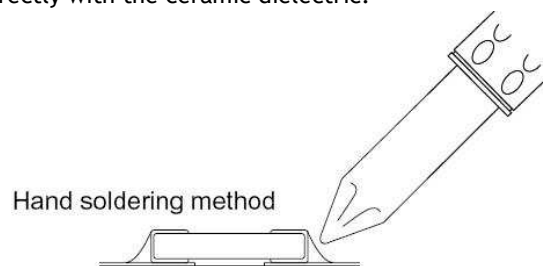
6-7 Solder repair by solder iron

1) Selection of the soldering iron tip

Tip temperature of solder iron varies by its type, P.C. board material and solder pad size. Higher tip temperature may be faster, but the heat shock may crack the chip capacitor. (Following conditions are recommended.)

Temp. ($^{\circ}\text{C}$)	Wattage (W)	Shape (mm)
300 Max	20 Max	$\Phi 3.0$ Max

2) Direct contact of the soldering iron with ceramic dielectric of chip capacitor may cause cracking. Do not make contact directly with the ceramic dielectric.



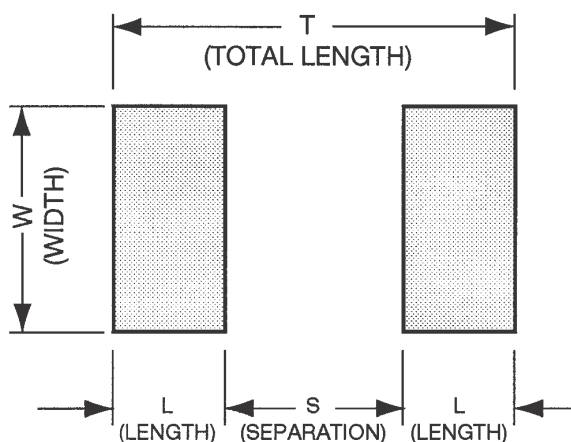


APPLICATION INFORMATION ON SOLDER PAD DESIGN FOR SURFACE MOUNT CHIP CAPACITOR

Recommended Pad Dimensions

Chip Size	Dimensions (inches)			
	L	W	S	T
0402*	0.021	0.022	0.017	0.059
0603*	0.035	0.030	0.030	0.100
0805	0.040	0.050	0.040	0.120
1206	0.040	0.065	0.080	0.160
1210	0.040	0.100	0.080	0.160
1812*	0.050	0.120	0.130	0.230
1825*	0.050	0.250	0.130	0.230
2220	0.050	0.250	0.130	0.230
2225*	0.050	0.250	0.170	0.270
3640*	0.060	0.400	0.300	0.420

*These sizes are recommended for use with IR and vapor phase soldering only.



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