WT8043

Synchronous Signal discriminator
for Multi-Sync Display Monitor

Jan. 30, 1996

Description

The WT8043 is a silicon monolithic circuit designed for synchronous signal processing of multi-sync display monitors capable of coping with many kinds of PC's and workstations. It can be applied to display monitors supporting standard IBM VGA, VESA super VGA and IBM 8514/A video modes. It can also be used in other high-end display monitors supporting non-standard video modes with user-defined horizontal/vertical frequency ranges.

WT8043 incorporates many functional circuits, horizontal/vertical frequency discrimination, display mode selection, and synchronous pulse polarity detection, into a single chip. Therefore, by using WT8043, monitor makers can shrink the PC board size, reduce the material cost with fewer components, and reduce labor cost as well.

Features

- Accepting separate H&V Synchronous signals with any polarities
- Support VESA VGA (640x480, 640x400, 640x350), VESA SVGA (800x600), European SVGA (800x600), VESA new SVGA (800x600), XGA (1024x768) and 1280x1024.
- Also including NEC (24K) mode, 3 VESA New 75Hz timing modes and Apple MAC II (35k) mode.
- Capable of processing horizontal frequency from 25KHz to 80KHz
- Capable of processing vertical frequency from 50Hz to 120Hz
- Standard IBM video mode control outputs (1024x768, 640x480, 640x400, 640x350)
- Six non-standard horizontal frequency control outputs with predefined frequency range. (users can define their own horizontal frequency range)
- Fixed polarity horizontal and vertical synchronous signals output
- Power supply voltage: 5V, but mode select control output and frequency discrimination control output, these open collector outputs can be combined with pull high resistor, pull up to 12V.

Application

- Auto size control for Multi-Sync Display Monitors

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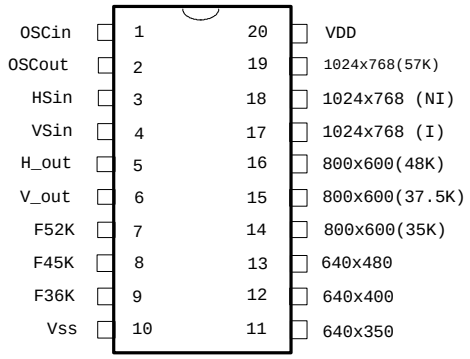
Ordering Information

Part No.	WT8043N16	WT8043N20P1	WT8043N20P4	WT8043N20P7	WT8043N20P8	WT8043N24
Package	P-DIP 16L	P-DIP 20L	P-DIP 20L	P-DIP 20L	P-DIP 20L	P-DIP 24L (skinny type)

Pin Configuration

WT8043N20P1



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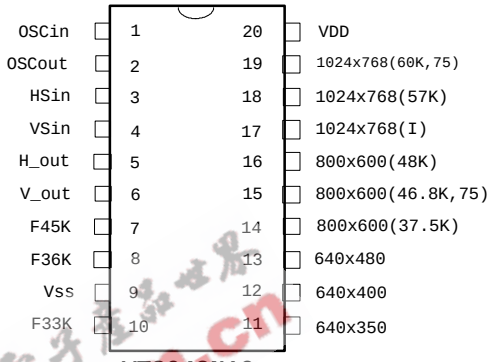

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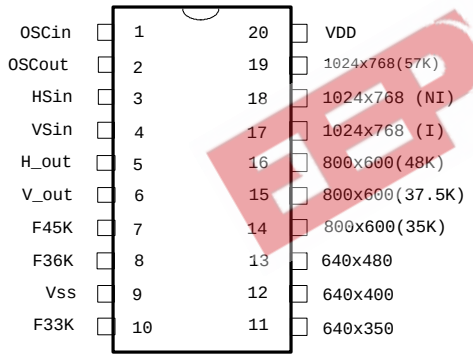
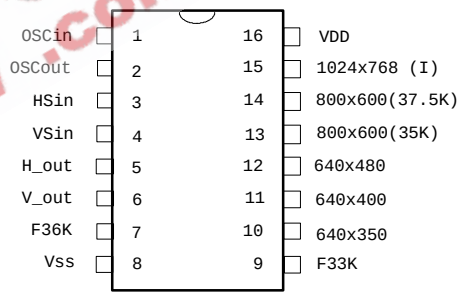


WT8043N16



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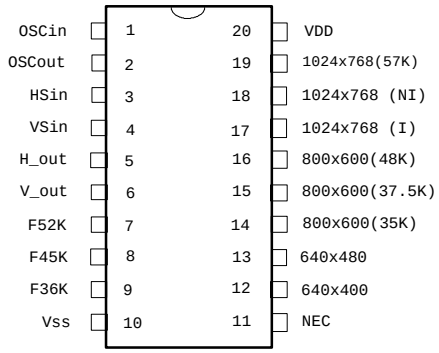

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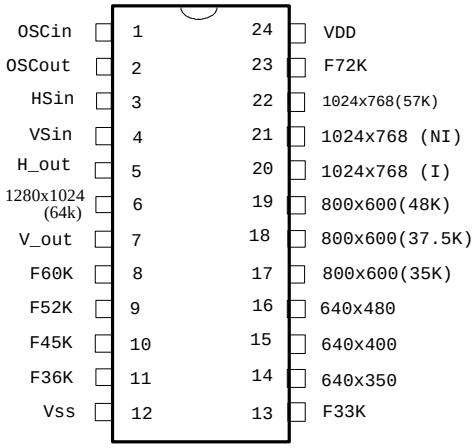
WT8043N24



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Absolute Maximum Ratings

Item	Symbol	Value	Unit
Digital Supply Voltage	V_{DD}	5.5	V
Horizontal Sync. Input Voltage	V_{HS}	V_{DD}(5)+0.3	V
Vertical Sync. Input Voltage	V_{VS}	V_{DD}(5)+0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{OPT}	0~70	°C
Storage Temperature Range	T_{STG}	-40~125	°C

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Digital Supply Voltage	V_{DD} (5)	4.5	5	5.5	V
Supply Current (Oscillator on)	I_P				mA
Synchronous Input Voltage Low	V_{IL}			0.8	V
Synchronous Input Voltage High	V_{IH}	2.4	4	5.0	V
Horizontal Synchronous Frequency Range	F_H	25	-	80	KHz
Vertical Synchronous Frequency Range	F_V	50	-	120	Hz
Crystal Clock Frequency	F_{CLK}	3.5764	3.58	3.5836	MHz
Open Drain Pull High Voltage	V_{OH}		8	12	V

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Electrical Characteristics

(V_{DD}=5V, T_{OPT}=25°C, Crystal=3.58MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Discrimintaion of H. Synchronous Frequency	F33K	32.95	-	33.05	KHz
	F36.2K	36.15	-	36.25	KHz
	F45K	44.95	-	45.05	KHz
	F52K	51.95	-	52.05	KHz
	F62K	61.95	-	62.05	KHz
	F72K	71.95	-	72.05	KHz
Output Low (H-out, V-out) When I_{OL} = 4mA	V_{OL1}			0.4	V
Output High (H-out, V-out) When I_{OH} = -400µA	V_{OH1}	2.4			V
Open Collector Output Low When I_{OL} = 6mA	V_{OL2}			0.4	V
Output Sink Current (H-out, V-out) When V_{OL1}= 0.4V	I_{OL1}			4	mA
Output Drive Current (H-out, V-out) When V_{OH1}= 2.4V	I_{OH1}			400	µA
Open Drain Sink Current When V_{OL2}= 0.4V	I_{OL2}			6	mA
Input H_SYNC Pulse Width	W_{H_SYNC}	0.56		4	µS
Input V_SYNC Pulse Width	W_{V_SYNC}	0.56		833	µS
H_SYNC, Output Pulse delay, respect to Hsin	T_{DHS}			60	nS
V_SYNC, Output Pulse delay, respect to Vsin	T_{VHS}			60	nS
Upper Trigger Input Point (H_IN, V_IN)	V_{UTP}	2.0			V
Lower Trigger Input Point (H_IN, V_IN)	V_{LTP}			0.8	V
Noise Margin (H_IN, V_IN)	V_{NM}			1.75	V

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Application Information

Name	Function	Structure of Terminal
OSCin	A clock generating circuit is built into the chip. So if a resonator is connected to OSCin / OSCout, a clock signal can be obtained	I
OSCout	Referent to OSCin pin	
HSin	Input terminal of horizontal synchronous Signal	I, TTL Compatible
VSin	Input terminal of vertical synchronous Signal	I, TTL Compatible
H_out	Output pin, active low, fixed polarity of original H_sync signal w/ same pulse width	O, TTL Compatible
1280 x 1024	1280x1024 mode control output	O, open drain
V_OUT	Output pin, active low, fixed polarity of original V_sync signal w/ same pulse width	O, TTL Compatible
F60K	H, frequency input 60k discrimination > 60k then active low, < 60k then high	O, open drain
F52K	> 52k then active low, < 52k then high	O, open drain
F45K	> 45k then active low, < 45k then high	O, open drain
F36K	> 36k then active low, < 36k then high	O, open drain
Vss	Ground	
F33K	> 33k then active low, < 33k then high	O, open drain
640 x 350	Mode seclect control output, if IBM VGA 640x350 mode, or VESA VGA 640x350 mode, then active low, else high state output	O, open drain

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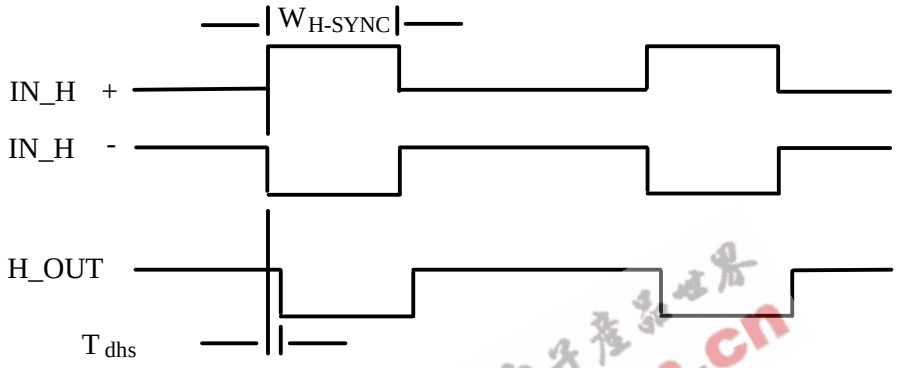
(Contd.)

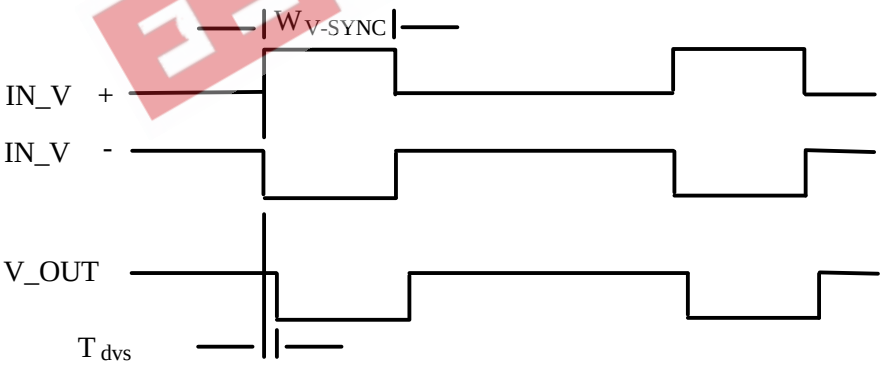
Name	Function	Structure of Terminal
NEC	NEC 640 x 400, 24.8kHz/ 56.4Hz timing mode	O, open drain
640 x 400	If IBM VGA 640 x 400 mode, or VESA VGA 640 x 400 mode then active "low"	O, open drain
640 x 480	If IBM VGA 640 x 480 mode, or VESA VGA 640 x 480 mode then active "low"	O, open drain
800 x 600	VESA super VGA mode Hsync freq. 35kHz	O, open drain
800 x 600	European super VGA mode Hsync freq. 37.5kHz	O, open drain
800 x 600 (46.8k,75)	VESA new 75Hz Timing mode	O, open drain
800 x 600	VESA new super VGA mode Hsync freq. 48kHz	O, open drain
1024x768 (I)	IBM 8514/A interlace mode	O, open drain
1024x768 (NI)	IBM 8514/A non-interlace mode	O, open drain
1024x768 (57k)	XGA 1024x768 mode Hsync freq. 57kHz	O, open drain
1024x768 (60k, 75)	VESA new 75Hz Timing mode	O, open drain
F72K	Hysnc freq. discrimination control output if > 72 kHz then active low, else high	O, open drain
VDD	5 Volts power supply	

Time Chart

- Hin - Hout



- Vin - Vout



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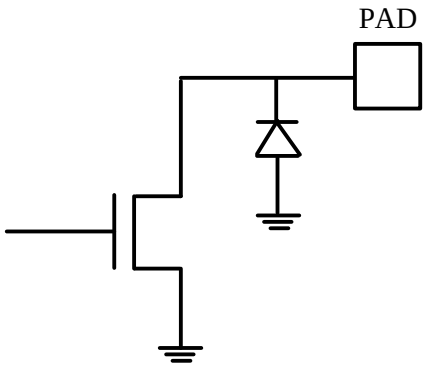
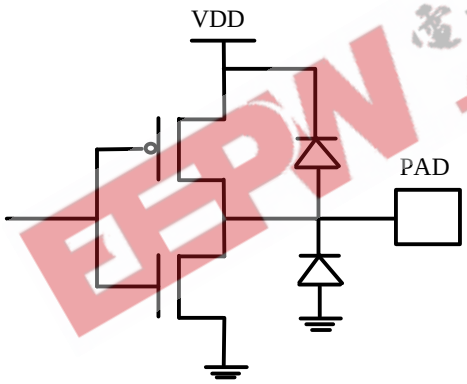
Structure of Terminal

Type 1



Open Drain NMOS can pull up by external resistor, no connector must be pull down or floating.

Type 2



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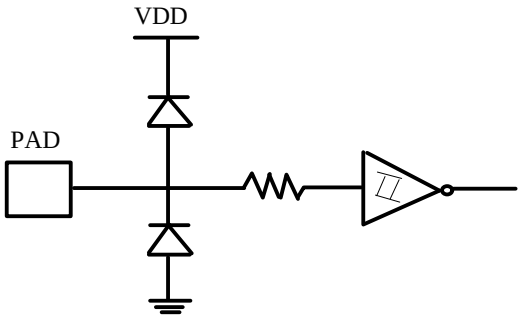

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Block Diagram I

Figure 1-1 WT8043N20P1 Functional Block Diagram

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Block Diagram II

Figure 1-2 WT8043N24 Functional Block Diagram

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Appication Description

General Description

Figure 1-1 and 1-2 is a simplified functional block diagram of the WT8043. It includes the following functional blocks: sync pulse polarity detector; horizontal and vertical frequency discriminator, mode selector.

The Sync pulse polarity detector accepts separete H and V sync signals with any polarities. It determines their polarities and sends the polarity information to the mode selector for video mode selection. It alos generates -H and -V signals in spite of their input polarities.

The H and V frequency discriminator determines the frequency range of H and V sync signals. The mode selector determines which operating video mode it should be, according to the frequency range and polarity of H and V sync signals. The operating video modes include the standard IBM VGA (640x350, 640x400, 640x480), super VGA (800x600) and IBM8514/A (Inerlaced, Non-interlaced), VESA VGA & SVGA mode, VESA new SVGA mode, XGA (1024x768), and 1280x1024 mode, also including NEC 24kHz and 3 VESA New 75Hz timing modes.

The mode selector also generates output signals that represent the frequency range of H. sync signal. The H sync signal is divided into 6 frequency ranges (3 ranges for WT8043N20) according to Fig. 2, WT8043 has preset the discriminating points between frequency ranges. However, it also offers the flexibility for providing user-defined discriminating points for non-standard video modes.

The digital noise filter is used for rejecting noise on the incoming horizontal and vertical synchronous signals. The input section uses two techniques to improve noise rejec-tion. So the low level noise and the large short duration noise spikes will be rejected. Horizontal synchronous pulse width under 0.56 μs and vertical synchronous pulse width under 0.56 μs will be considered as noise.

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H/V Frequency Divisions and Video Modes

Figure 2 illustrates the typical frequency ranges of H and V sync signals for display monitors. The operating video modes are determined by the H and V frequencies, and occasionally, by their polarities. The typical video modes of display monitors include the NEC 24k mode, IBM VGA, VESA VGA, European VGA/Super VGA, Apple MAC II, VESA Super VGA, IBM 8514/A,3 VESA New 75Hz modes, XGA, and 1280x 1024.

WT8043 can determine 18 standard video modes (as shown in Table 1) according to H and V frequencies and polari-ties. These standard video modes include the IBM VGA, VESA VGA, VESA super VGA and IBM 8514/A. This provides the users with the capability to adjust the screen size for different modes.

WT8043 pre-sets the discriminating points both on H and V frequencies. The discriminating points for H sync are 33KHz, 36.2KHz, 45KHz, 52KHz, 62KHz and 72KHz. These discriminating points will be able to identify various video modes as shown in Fig. 2. WT8043 also provides the flexibility for users to define these discriminating points through mask option.

The tolerance for H sync frequency discrimination is 0.05KHz. For instance, the 33KHz discriminating point will be able to distinguish the H sync frequency that is either "less than or euqal to" 32.95KHz, or "greater than or equal to" 33.05KHz. There is an ambiguous region between 32.95KHz and 33.05KHz.

WT8043 has three discriminating points, 64Hz, 73.5Hz and 78Hz, for the V sync signal as shown in Fig.2. The tolerance is 0.01Hz. The discrimination results of V sync frequency are used internally for mode selection.

Base on the package consideration, IBM VGA mode and VESA VGA mode (both have same resolution: 640x480, 640x400, 640x350) are decoded on same open Drain structure output pins (e.g. pin 14 to pin 16 for N20P1 pin type package). In case of these whole 6 modes decoding is needed, the horizontal frequency discrimination pin F33k or F36k must take into consideration. The horizontal frequency of IBM VGA mode is 31.4kHz, and VESA IBM VGA mode is 37.5kHz. Using F33k or F36k pin can clearly identify these two standard modes. The decoding circuit is attached on application section for reference.

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Table 1: Graphaic Standard and Frequencies

¡ I

Graphic Standard	Resolution	Horizontal	Vertical	Polarities
NEC Timing	640 x 400	24.8KHz	56.4Hz	-,-
IBM VGA	640 x 350	31.5KHz	70Hz	+,-
	640 x 400	31.5KHz	70Hz	-,+
	640 x 480	31.5KHz	60Hz	-,-
Mac II	640 x 480	35.0KHz	67Hz	
New 72Hz	640 x 480	38.6KHz	72Hz	-,+
VESA Super VGA	800 x 600	35.2KHz	56Hz	
IBM 8514/A interlaced	1024 x 768	35.5KHz	86Hz	
VESA VGA	640 x 350	37.5KHz	83Hz	+,-
	640 x 400	37.5KHz	83Hz	-,+
	640 x 480	37.5KHz	72Hz	-,-
VESA New 75Hz Timing	640 x 480	37.5KHz	75Hz	-,-
European Super VGA	800 x 600	37.5KHz	60Hz	
VESA New 75Hz Timing	800 x 600	46.8KHz	75Hz	
VESA New Super VGA	800 x 600	48.0KHz	72Hz	
IBM 8514/A Non-interlaced	1024 x 768	48.5KHz	60Hz	
VESA New 1024 x 768	1024 x 768	56.5KHz	72Hz	
VESA New 75Hz Timing	1024 x 768	60.0KHz	75Hz	
Work Station 1280 x1024	1280 x 1024	64.0KHz	60Hz	

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Figure 2: H/V Frequency Division and Video Mode

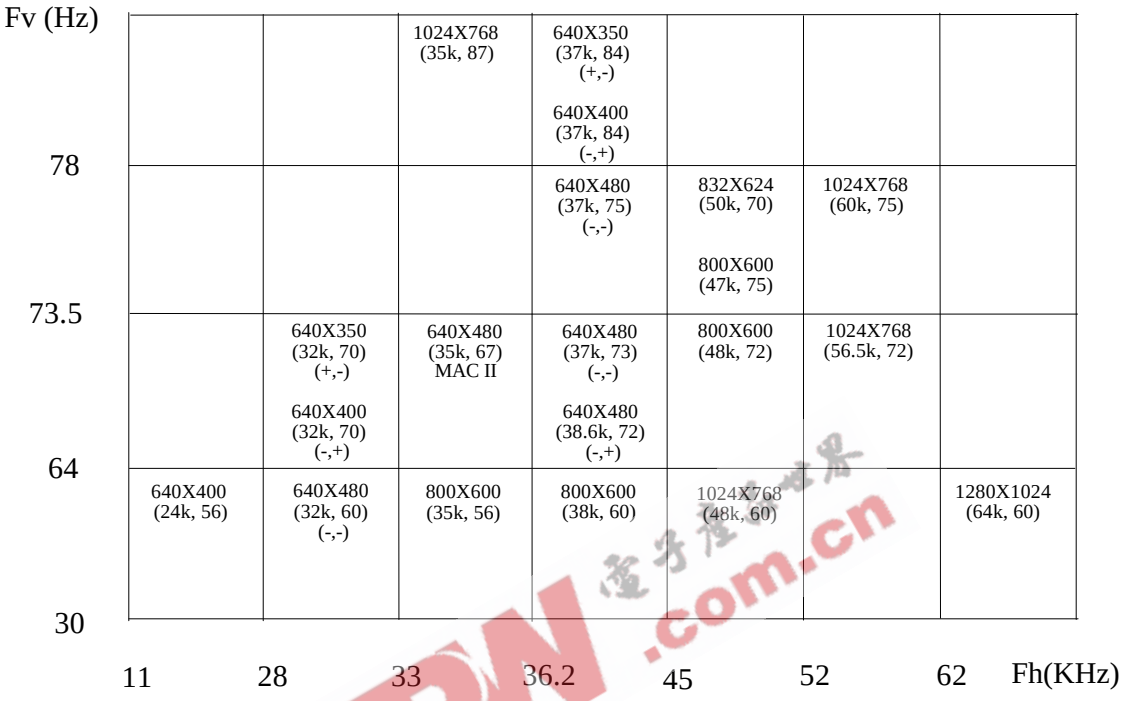

Table 2: IBM VGA/ VESA VGA Decoding Table

Mode	PIN	640 x 480	640 x 400	640 x 350
IBM VGA	640 x 480	0	1	1
	640 x 400	1	0	1
	640 x 350	1	1	0
VESA VGA	640 x 480	0	1	1
	640 x 400	1	0	1
	640 x 350	1	1	0

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Horizontal Frequency Discriminator

There are 3 horizontal frequency discriminator pins on 20 pin type package: 36.2kHz, 45kHz, 52kHz (for N20P1), 33kHz, 36.2kHz, 45kHz (for N20P4); 2 frequency discriminator pins on 16 pin type package: 33kHz, 36.2kHz and 6 frequency discriminator pins on 24 pin type package: 33kHz, 36.2kHz, 45kHz, 52kHz, 62kHz and 72kHz. Please refer to table 3 for the logical truth table of these pins. These frequency discriminator pins can pull up to +12V through a resistor, sink current to the open drain structure must keep under 6mA (ref. P4 Electrical Characteristics). These frequency discriminator pins output can be used for CS Capacitor Control directly as well as other application.

Table 3: Truth table of Frequency discriminator

Signal / Hsync	F33K	F36.2K	F45K	F52K	F62K	F72K
Hs < 33k	1	1	1	1	1	1
36.2k > Hs > 33k	0	1	1	1	1	1
45k > Hs > 36.2k	0	0	1	1	1	1
52k > Hs > 45k	0	0	0	1	1	1
62k > Hs > 52k	0	0	0	0	1	1
72k > Hs > 62k	0	0	0	0	0	1
Hs > 72k	0	0	0	0	0	0

SYNC Output State Description

Both H_out / V_out duplicate Hsin/Vsin in the same frequency and pulse width, but are fixed at negative polarity. And H_out/ V_out have their own cut-off frequency: 15kHz for H_Sync and 30Hz for V_Sync. While the frequency of input signal is less than the cut-off frequency, the output will keep in low state. Please refer to the Table 4.

Table 4:

Hsin	Vsin	H_out	V_out
>15kHz	>30Hz	Negative polarity Hsin	Negative polarity Vsin
>15kHz	<30Hz	Negative polarity Hsin	Low state
<15kHz	>30Hz	Low state	Negative polarity Vsin
<15kHz	<30Hz	Low state	Low state

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Application Circuit I

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Application Cirucit II

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Physical Dimension

	A	B	C	D	E	F	G
16L	754	250	130	100	130	355	300
20L	1024	250	130	100	130	355	300
24L skinny	1250	260	130	100	130	355	300

* Dimension in mil
* 1mm = 39.37 mil

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