MTP15N06E

Motorola Preferred Device

Designer's™ Data Sheet

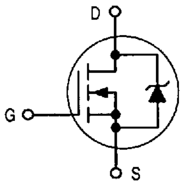
TMOS E-FET™ Power Field Effect Transistor

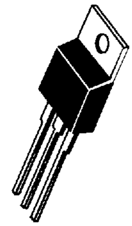
N–Channel Enhancement–Mode Silicon Gate

TMOS POWER FET
15 AMPERES
$R_{DS(on)}$ = 0.12 OHM
60 VOLTS

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

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MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Pulsed (tp ≤ 10 μs)	I_D I_D I_{DM}	15 10 40	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.5	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vpk, I_L = 15 Apk, L = 0.98 mH, R_G = 25 Ω)	E_{AS}	110	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	60 —	— 64	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	— 6.0	4.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$R_{DS(on)}$	—	0.1	0.12	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 15 Adc) (I_D = 7.5 Adc, T_J = 150°C)		$V_{DS(on)}$	— —	— —	2.16 1.8	Vdc
Forward Transconductance (V_{DS} ≥ 8.0 Vdc, I_D = 7.5 Adc)		g_{FS}	4.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	500	800	pF
Output Capacitance		C_{oss}	—	240	350	
Transfer Capacitance		C_{rss}	—	60	150	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 15 Adc, V_{GS} = 10 Vdc, R_G = 9.0 Ω)	$t_{d(on)}$	—	8.0	16	ns
Rise Time		t_r	—	70	140	
Turn–Off Delay Time		$t_{d(off)}$	—	16	35	
Fall Time		t_f	—	40	80	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 15 Adc, V_{GS} = 10 Vdc)	Q_T	—	15	35	nC
		Q_1	—	4.0	—	
		Q_2	—	7.0	—	
		Q_3	—	6.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 15 Adc, V_{GS} = 0) (I_S = 15 Adc, V_{GS} = 0, T_J = 150°C)	V_{SD}	— —	1.1 0.97	1.6 —	Vdc
Reverse Recovery Time	(I_S = 15 Adc, dI_S/dt = 100 A/μs)	t_{rr}	—	70	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured fromthe drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs max, Duty Cycle = 2.0%.
(2) Switching characteristics are independent of operating junction temperature.

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TYPICAL ELECTRICAL CHARACTERISTICS

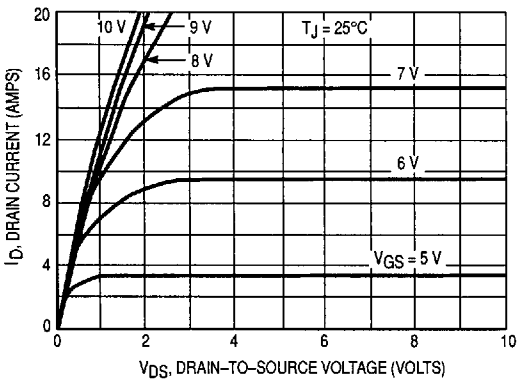

Figure 1. On–Region Characteristics

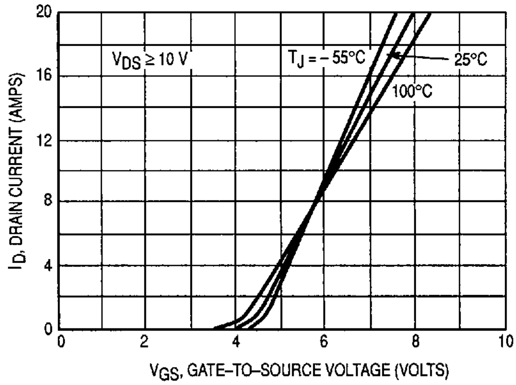

Figure 2. Transfer Characteristics

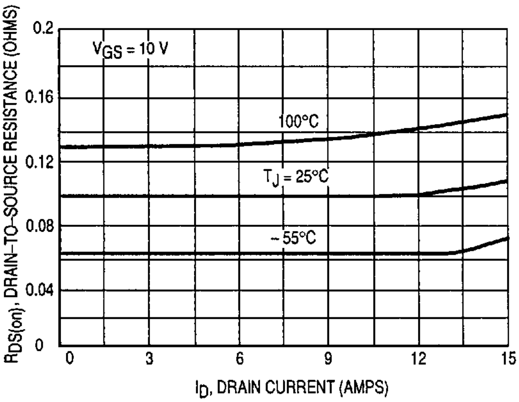

Figure 3. On–Resistance versus Drain Current

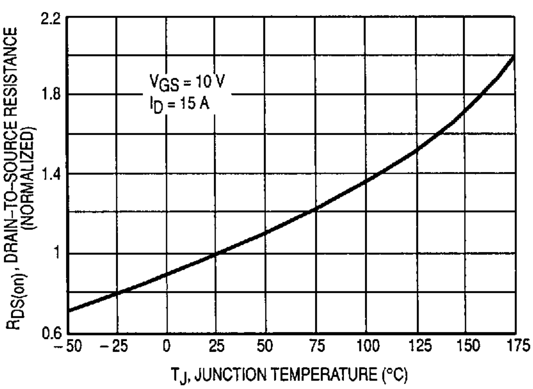

Figure 4. On–Resistance Variation With Temperature

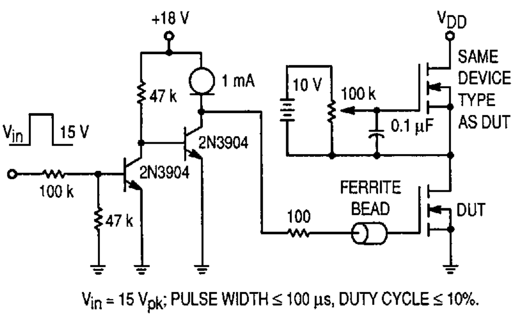

Figure 5. Gate Charge Test Circuit

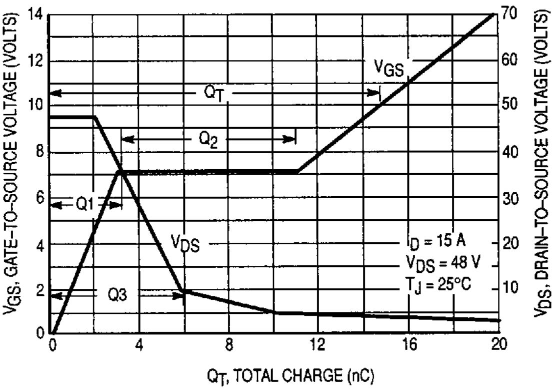

Figure 6. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

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SAFE OPERATING AREA INFORMATION

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 175°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance–General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, BV_{DSS}. The switching SOA shown in Figure 9 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

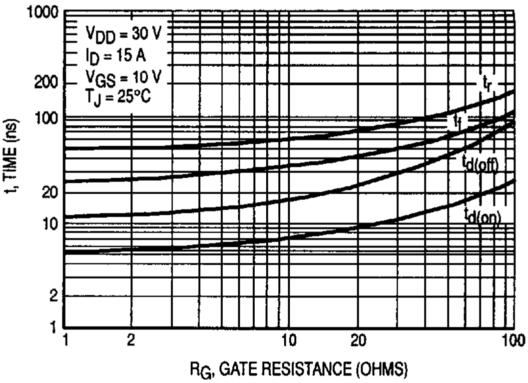

Figure 7. Resistive Switching Time Variation versus Gate Resistance

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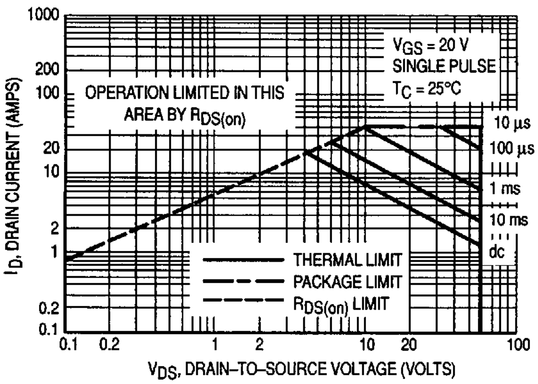

Figure 8. Maximum Rated Forward Biased Safe Operating Area

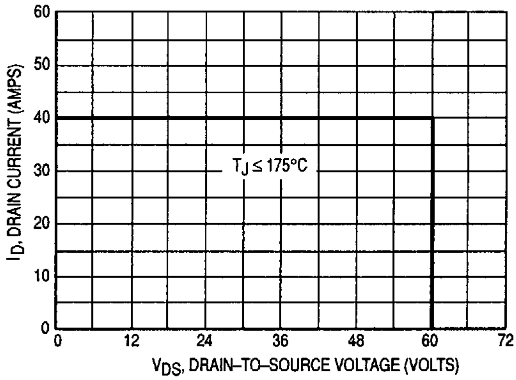

Figure 9. Maximum Rated Switching Safe Operating Area

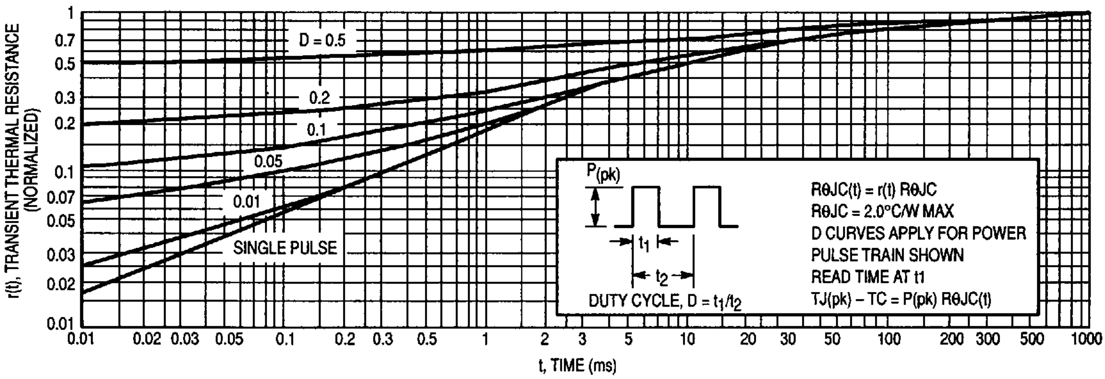

Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source–drain current versus re–applied drain voltage when the source–drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half–bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source–drain diode current just prior to the onset of commutation.

V_R is specified at rated $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/µs.

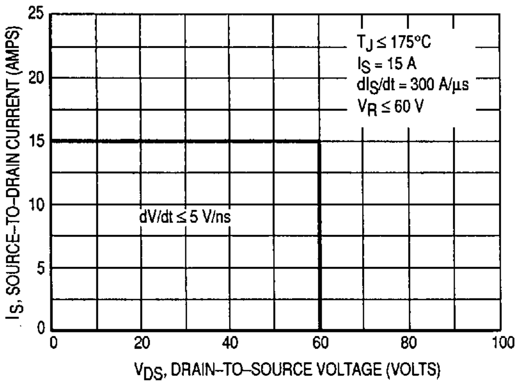

Figure 12. Commutating Safe Operating Area (CSOA)

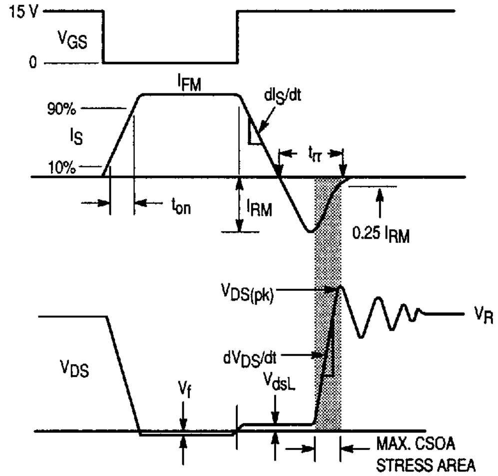

Figure 11. Commutating Waveforms

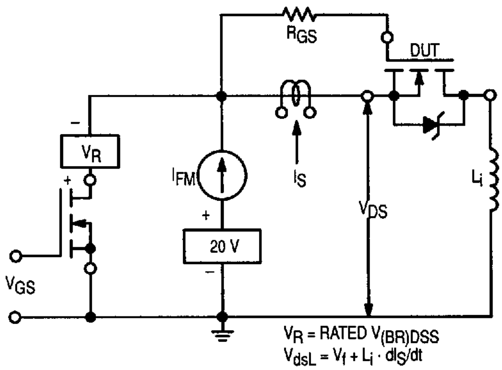

Figure 13. Commutating Safe Operating Area Test Circuit

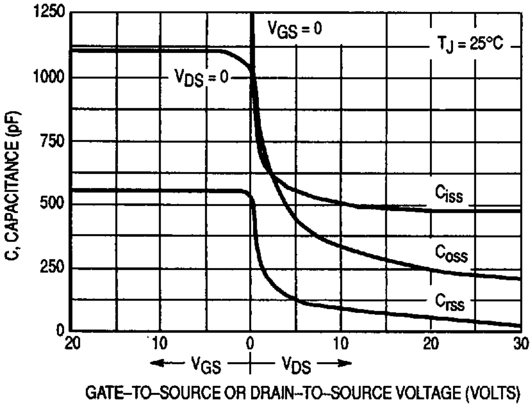

Figure 14. Capacitance Variation

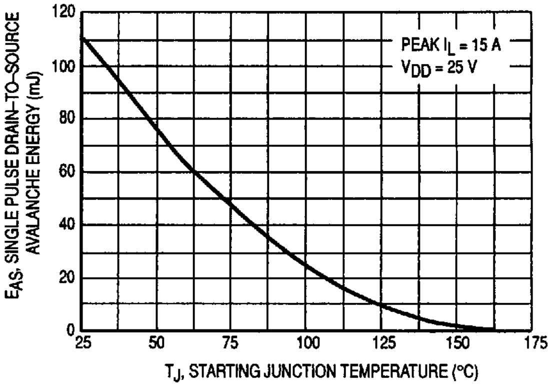

Figure 15. Maximum Avalanche Energy versus Starting Junction Temperature

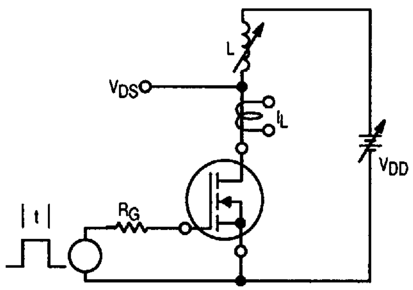

Figure 16. Unclamped Inductive Switching Test Circuit

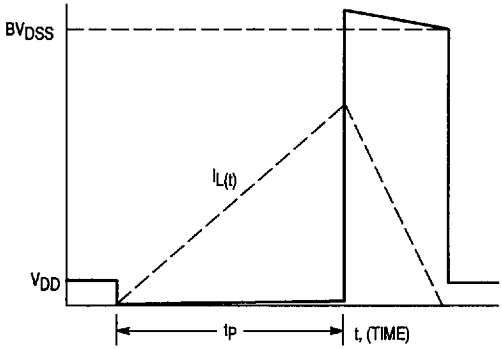

Figure 17. Unclamped Inductive Switching Waveforms

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