

TTL to Differential LVPECL Translator

Applications

- PECL clock source

General Description

The TLSI T73LVP10 is a general purpose TTL (CMOS) to differential LVPECL translator operating from a single 3.3V supply. The device accepts LVTTTL or LVCMOS input and provides differential LVPECL outputs referenced to the positive supply rail.

Features

- 350pS typical propagation delay
- Differential LVPECL outputs
- Flow-through pinout
- -40 °C to +85 °C operating temperature range
- ESD rating >2000V (Human Body Model) or >200V (Machine Model)
- Available as die, in 6-pin SOT package or 8-pin SOIC package

Figure 1. Functional Block Diagram & Pin Assignment

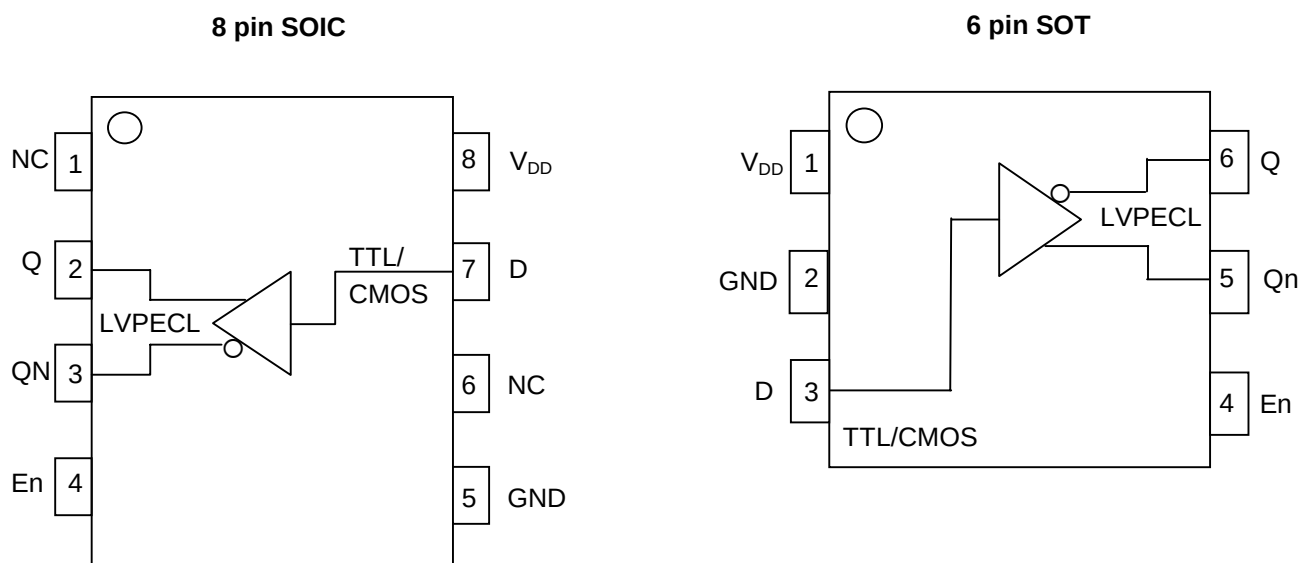


Table 1. Pin Description

Name	Description	Type	8-SOIC Pin #	6-SOT Pin #
NC	No Connection	-	1, 6	
Q	PECL data output	O	2	5
QN	PECL complementary data output	O	3	6
V _{DD}	Connect to 3.3V	P	8	1
D	CMOS/TTL data input	I	7	3
GND	Connect to ground	P	5	2
EN	TTL/CMOS active LOW enable input with pull-down resistor		4	4

Legend: I = Input
O = Output
P = Power supply connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{DD}	Supply voltage	Referenced to GND			4.6	V
V _{IN}	Input voltage	Referenced to GND	-0.5		V _{DD}	V
I _{OUT}	Output current in LOW state				50	mA
T _{STG}	Storage temperature		0		150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{DD}	Power Supply Voltage		3.0		3.6	V
T _A	Ambient Temperature		-40		85	°C
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
t _{Rin}	Input rise time	10% to 90%	1			V/ns
t _{Fin}	Input fall time	90% to 10%	1			V/ns

Table 4. DC Characteristics

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 3.0\text{V}$ to 3.6V unless otherwise stated below.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I _{IH}	Input HIGH Current	V _{IN} = 2.7V				20	μA
I _{IL}	Input LOW Current	V _{IN} = 0.5V				-20	μA
V _{IK}	Input Clamp Diode Voltage	I _{IN} = -18mA				-1.2	V
V _{OH}	Output HIGH Voltage ^(1, 2)	-40°C	V _{DD} = 3.3V	2.05	2290	2415	mV
		25°C		2.05	2355	2480	mV
		85°C		2.05	2415	2540	mV
V _{OL}	Output LOW Voltage ^(1, 2)	-40°C	V _{DD} = 3.3V	1365	1490	1615	mV
		25°C		1430	1555	1680	mV
		85°C		1490	1615	1740	mV
I _{DD}	Power Supply Current				28		mA

Notes: 1. The T73LVP10 is designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board.
 2. Q and QN outputs are loaded with 50 ohms to $V_{DD}-2$ volts.

Table 5. AC Characteristics

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 3.0\text{V}$ to 3.6V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay ⁽¹⁾			0.35	0.9	ns
t_{PHL}	Propagation Delay ⁽¹⁾			0.35	0.9	ns
t_r/t_f	Output Rise/Fall time	20-80%	0.25	0.3	0.7	ns
f_{MAX}	Maximum Input Frequency	LVTTL or LVCMOS input		400		MHz
f_{MAX}	Maximum Input Frequency ⁽²⁾	750mV peak-to-peak sine wave centered around 1.5V		500		MHz

Notes: 1. Q and QN outputs are loaded with 50 ohms to $V_{DD}-2$ volts.
 2. Measured using a 750mV peak-to-peak, 50% duty cycle clock source.

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T737LVP10S1	T73P10S1	Tubes	8	SOIC	-40°C to +85°C
T73LVP10S1X	T73P10S1	Tape & Reel	8	SOIC	-40°C to +85°C
T73LVP10S2	T73P10S2	Tubes	6	SOT	-40°C to +85°C
T73LVP10S2X	T73P10S2	Tape & Reel	6	SOT	-40°C to +85°C
T73LVP10/D		Dice			-40°C to +85°C