PO100HSTL11A

2.3V - 3.6V 1 to 2 Differential Clock/Data Fanout Buffer

1.24GHz Noise Cancellation TTL/CMOS Potato Chip

FEATURES:

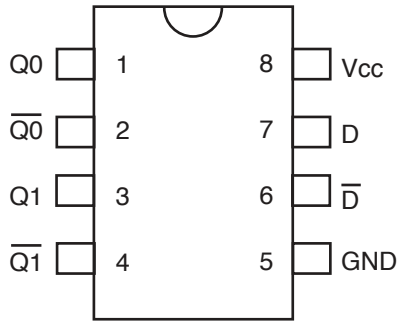
- Patented Technology
- Two HSTL differential outputs
- One pair of LVDS/LVPECL/HSTL/ differential or single-ended inputs
- Operating frequency up to 1.24GHz with 2pf load
- Operating frequency up to 900MHz with 5pf load
- Operating frequency up to 400MHz with 15pf load
- Very low output pin to pin skew < 40ps
- Propagation delay < 2.0ns max with 15pf load
- 2.3V to 3.6V power supply
- Industrial temperature range: –40°C to 85°C
- Available in 8-pin SOIC package
- Available in 8-pin TSSOP package

DESCRIPTION:

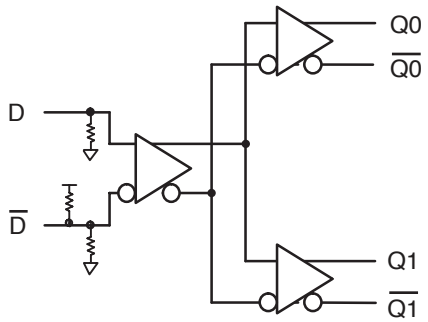
Potato Semiconductor's PO100HSTL11A is designed for world top performance using submicron CMOS technology to achieve 1.24GHz HSTL output frequency with less than 2.0ns propagation delay.

The PO100HSTL11A is a low-skew, 1-to-2 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 1.24GHz .

Pin Configuration



Logic Block Diagram



Pin Description

PIN	FUNCTION
D, $\overline{D}$	LVDS LVPECL HSTL Inputs
Q0, $\overline{Q0}$, Q1, $\overline{Q1}$	HSTL Outputs
V_{CC}	Positive Supply
GND	Ground Supply

1.24GHz Noise Cancellation TTL/CMOS Potato Chip

Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to Vcc	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:
stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			88		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			88		KΩ

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=12mA	-	0.3	0.5	V
V_{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	Vcc	V
V_{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I_{IH}	Input High current	Vcc = 3.6V and Vin = Vcc	-	-	1	uA
I_{IL}	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-1	uA
V_{IK}	Clamp diode voltage	Vcc = Min. And IIN = -18mA	-	-0.7	-1.2	V

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA

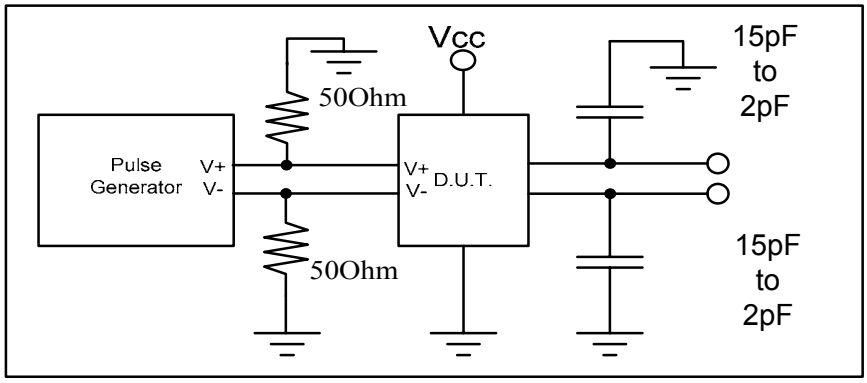
Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25•C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Switching Characteristics

Symbol	Description	Test Conditions (1)	Max	Unit
t_{PD}	Propagation Delay D to Output pair	CL = 15pF	2.0	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	ns
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	40	ps
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz	250	ps
fmax	Input Frequency	CL =15pF	400	MHz
fmax	Input Frequency	CL = 5pF	900	MHz
fmax	Input Frequency	CL = 2pF	1240	MHz

Notes:
1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

Test Circuit



1.24GHz Noise Cancellation TTL/CMOS Potato Chip

Test Waveforms

FIGURE 1. LVDS/ PECL/ ECL/ HSTL /DIFFERENTIAL INPUT WAVEFORM DEFINITIONS

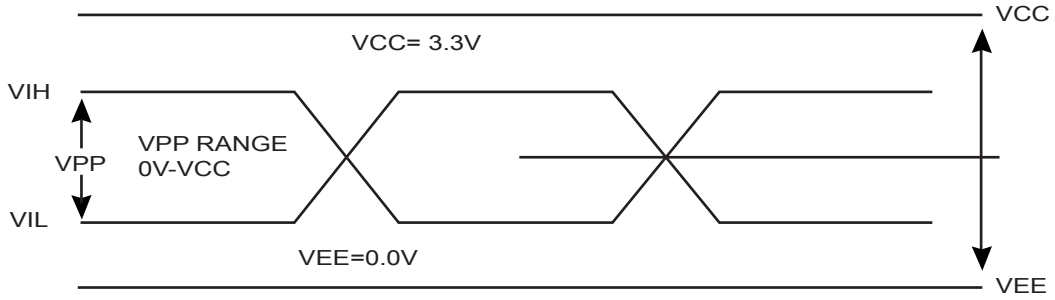


FIGURE 2. HSTL/HSTL OUTPUT

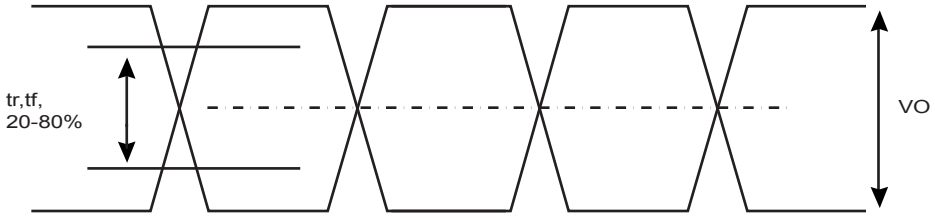
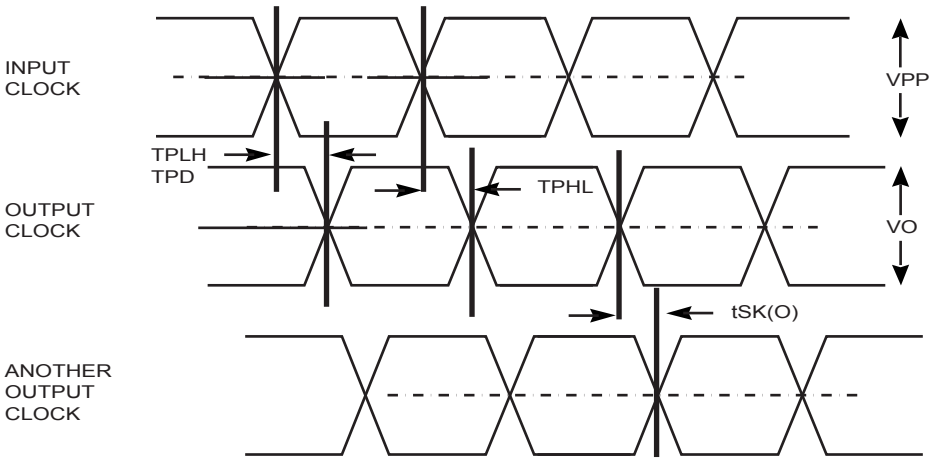
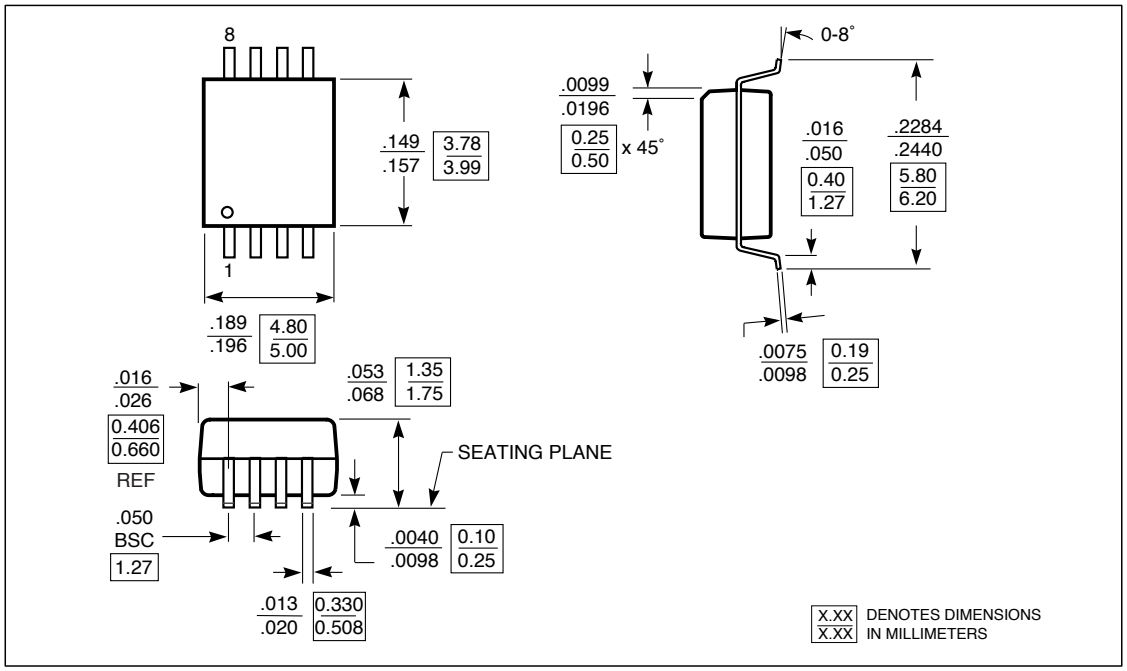


FIGURE 3. Propogation Delay, Output pulse skew, and output-to-output skew for D to output pair

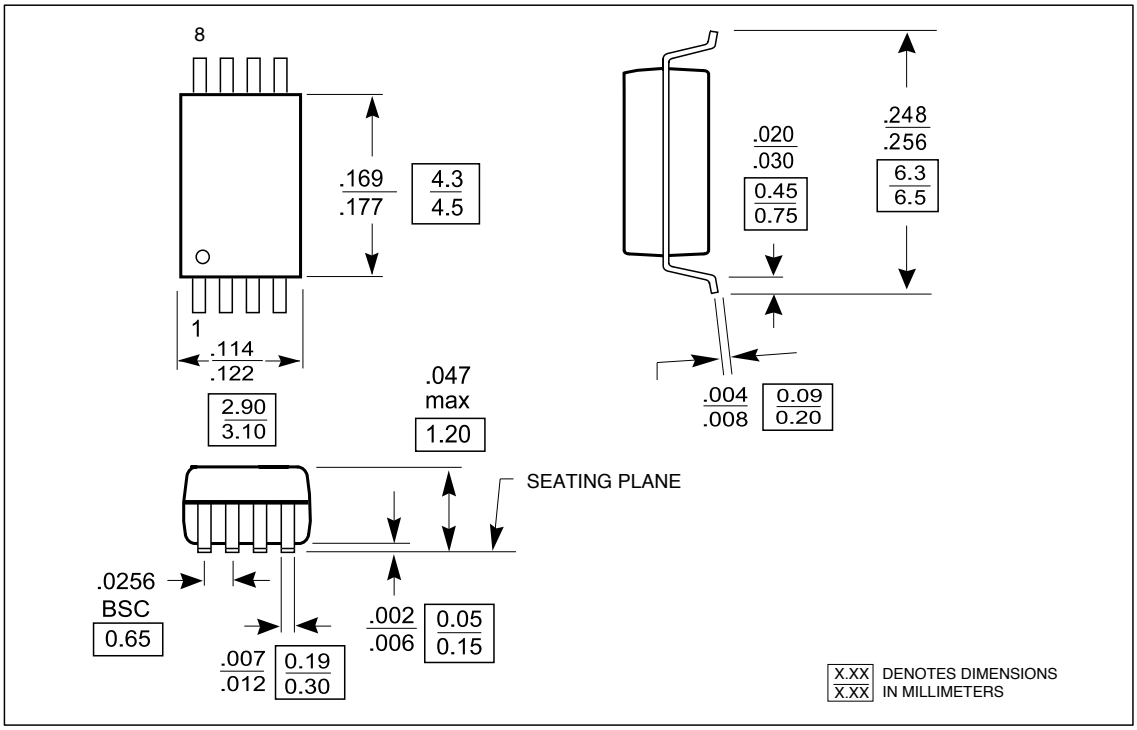


1.24GHz Noise Cancellation TTL/CMOS Potato Chip

Packaging Mechanical Drawing: 8 pin SOIC



Packaging Mechanical Drawing: 8 pin TSSOP



1.24GHz Noise Cancellation TTL/CMOS Potato Chip

IC Ordering Information

Ordering Code	Package		Top-Marking	T_A
PO100HSTL11ASU for Tube	8pin 150mil SOIC	Pb-free & Green	PO100HSTL11AS	-40°C to 85°C
PO100HSTL11ASR for Tape & Reel	8pin 150mil SOIC	Pb-free & Green	PO100HSTL11AS	-40°C to 85°C
PO100HSTL11ATU for Tube	8pin 150mil TSSOP	Pb-free & Green	PO100HSTL11AT	-40°C to 85°C
PO100HSTL11ATR for Tape & Reel	8pin 150mil TSSOP	Pb-free & Green	PO100HSTL11AT	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	TAPE & REEL PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER TAPE	TAPE LEADER LENGTH	QTY PER TUBE
S	8pin 150mil SOIC	12	8	Top Left Corner	39 (12″)	3000	64 (20″)	97
T	8pin 173mil TSSOP	12	8	Top Left Corner	39 (12″)	3000	64 (20″)	158