PO74G139A

DUAL2-LINETO4-LINEDECODER/DEMULTIPLEXER

74 Series Noise Cancellation GHz Logic

FEATURES:

. Patented technology
. Operating frequency up to 1.125GHz with 2pf load
. Operating frequency up to 800MHz with 5pf load
. Operating frequency up to 350MHz with 15pf load
. VCC Operates from 1.65V to 3.6V
. Propagation delay < 1.7ns max with 15pf load
. Low input capacitance: 4pf typical
. Available in 16 pin SOIC package

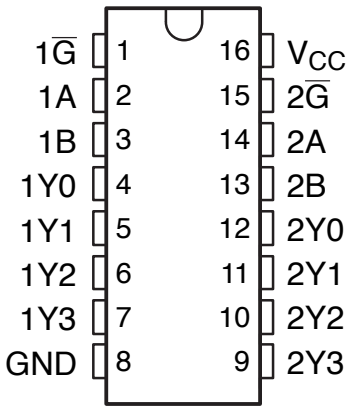
DESCRIPTION:

Potato Semiconductor's PO74G139A is designed for world top performance using submicron CMOS technology to achieve 1.125GHz TTL /CMOS output frequency with less than 1.7ns propagation delay. This quadruple bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation.

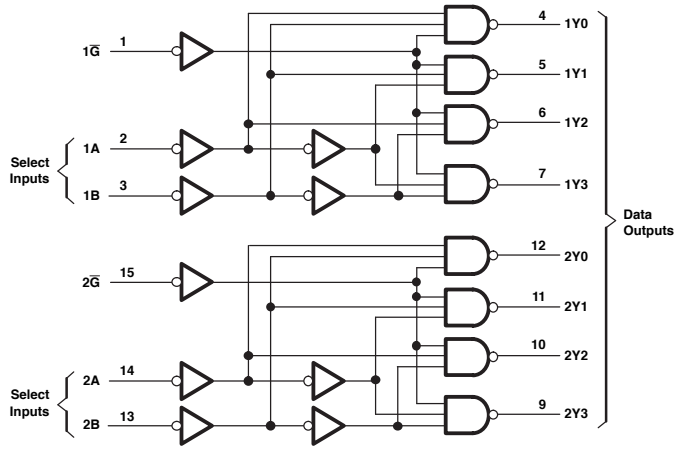
The PO74G139A comprises two individual 2-line to 4-line decoders in a single package. Theactive-lowenable ($\overline{G}$) input can be used as a data line in demultiplexing applications. This decoder/ demultiplexer features fully buffered inputs, each of which represents only one normalized-load to itsdriving circuit.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

Pin Configuration



Logic Block Diagram



Pin Description

INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y3	Y2	Y1	Y0
L	L	L	H	H	H	L
L	L	H	H	H	L	H
L	H	L	H	L	H	H
L	H	H	L	H	H	H
H	X	X	H	H	H	H

Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 125	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:
stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=12mA	-	0.3	0.5	V
V_{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	5.5	V
V_{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I_{IH}	Input High current	Vcc = 3.6V and Vin = 5.5V	-	-	1	uA
I_{IL}	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-1	uA
V_{IK}	Clamp diode voltage	Vcc = Min. And I_{IN} = -18mA	-	-0.7	-1.2	V

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA
ΔI_{CC}	Power Supply Current per Input High	Vcc=Max, Vin= Vcc-0.6V	-	50	300	uA

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Capacitance

Parameters (1)	Description	Test Conditions	Typ	Unit
Cin	Input Capacitance	Vin = 0V	4	pF
Cout	Output Capacitance	Vout = 0V	6	pF

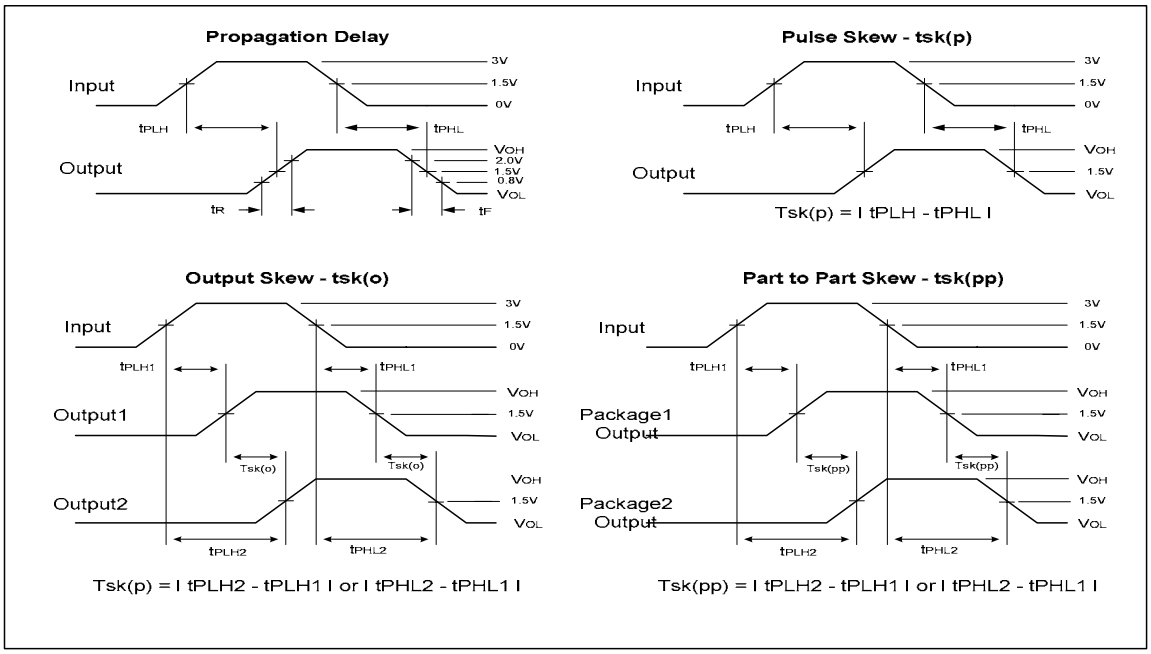
Notes:
1 This parameter is determined by device characterization but not production tested.

Switching Characteristics

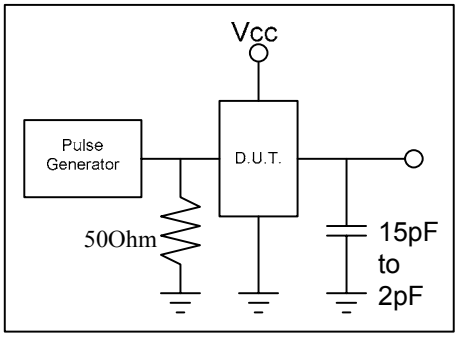
Symbol	Description	Test Conditions (1)	Max	Unit
t_{PLH}	Propagation Delay A, B to Y	CL = 15pF	1.7	ns
t_{PHL}	Propagation Delay A, B to Y	CL = 15pF	1.7	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	ns
tsk(o)	Output Pin to Pin Skew	CL = 15pF, 125MHz	0.25	ns
fmax	Input Frequency	CL =15pF	350	MHz
fmax	Input Frequency	CL = 5pF	800	MHz
fmax	Input Frequency	CL = 2pF	1125	MHz

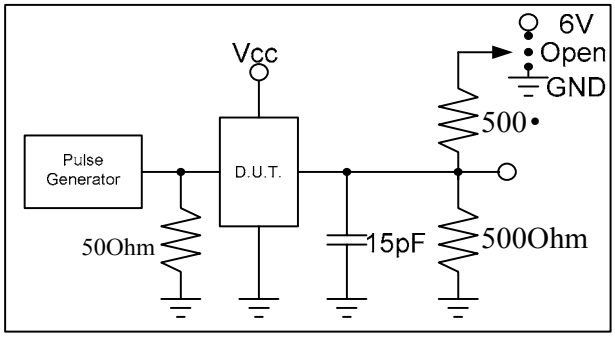
Notes:
1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

Test Waveforms

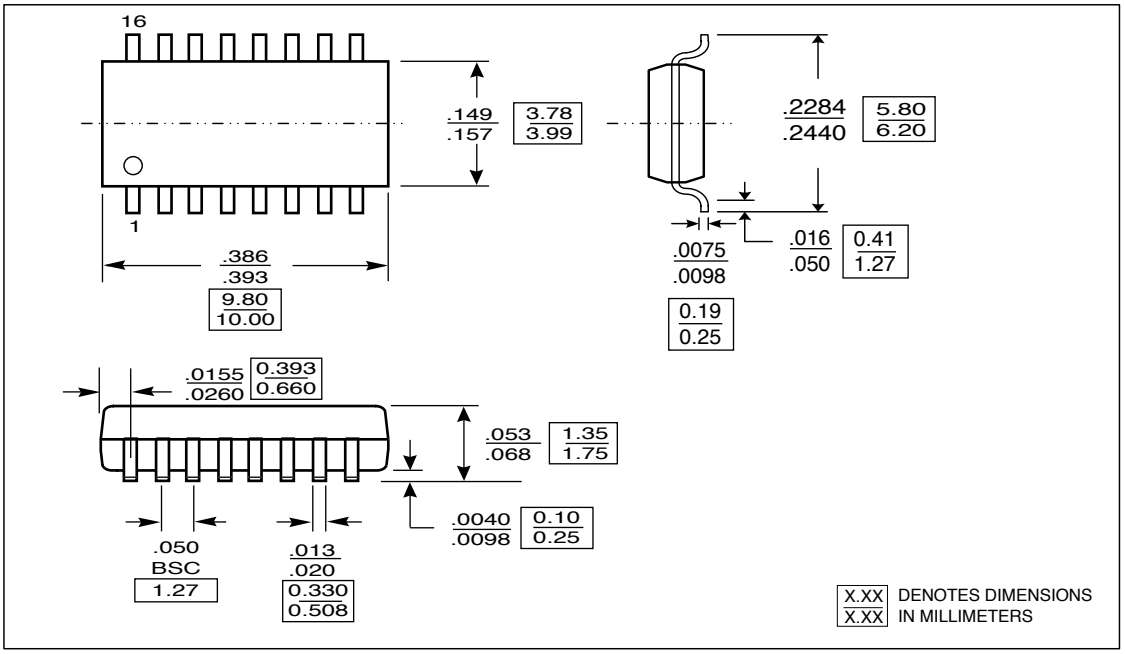


Test Circuit

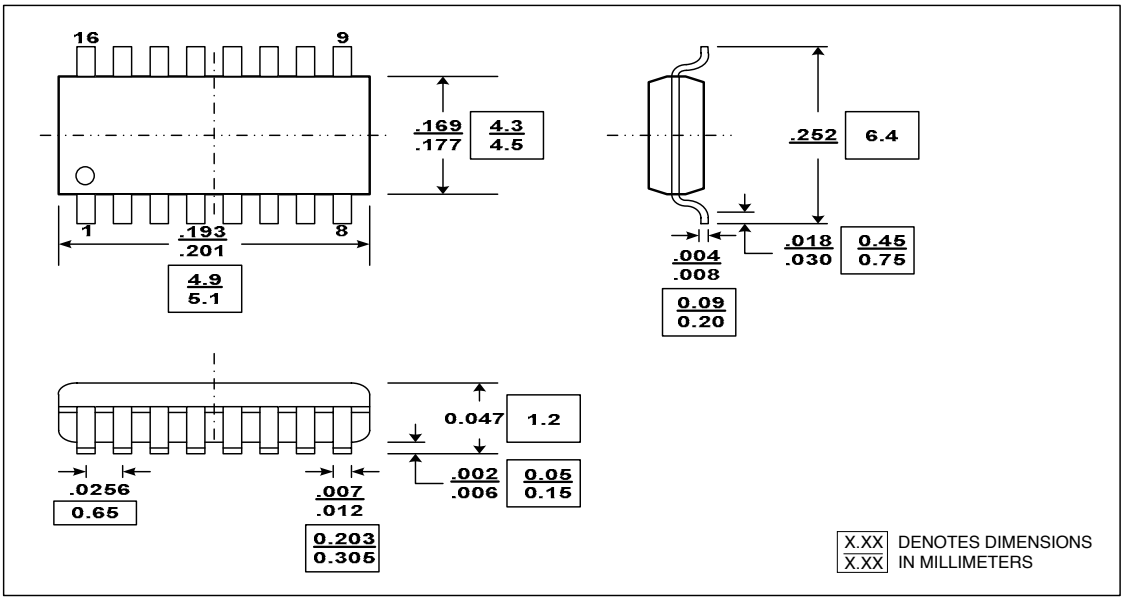




Packaging Mechanical Drawing: 16 pin SOIC



Packaging Mechanical Drawing: 16 pin TSSOP



IC Ordering Information

Ordering Code	Package		Top-Marking	T_A
PO74G139ASU for Tube	150mil SOIC 16	Pb-free & Green	POTATO74G139AS	-40°C to 85°C
PO74G139ASR for Tape & Reel	150mil SOIC 16	Pb-free & Green	POTATO74G139AS	-40°C to 85°C
PO74G139ATU for Tube	173mil TSSOP 16	Pb-free & Green	POTATO74G139AT	-40°C to 85°C
PO74G139ATR for Tape & Reel	173mil TSSOP 16	Pb-free & Green	POTATO74G139AT	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER REEL	TAPE LEADER LENGTH	QTY PER TUBE
S	SOIC 16	16	8	Top Left Corner	39 (12”)	3000	64 (20”)	48
T	TSSOP 16	12	8	Top Left Corner	39 (12”)	3000	64 (20”)	96