PO74G16241A

16-BIT BUFFERS/ DRIVERS WITH 3-STATE OUTPUTS

74 Series Noise Cancellation GHz Logic

FEATURES:

. Patented technology
. Operating frequency up to 1.125GHz with 2pf load
. Operating frequency up to 700MHz with 5pf load
. Operating frequency up to 300MHz with 15pf load
. Operating frequency up to 100MHz with 50pf load
. VCC Operates from 1.65V to 3.6V
. Propagation delay < 1.5ns max with 15pf load
. Low input capacitance: 4pf typical
. Available in 48pin TSSOP package

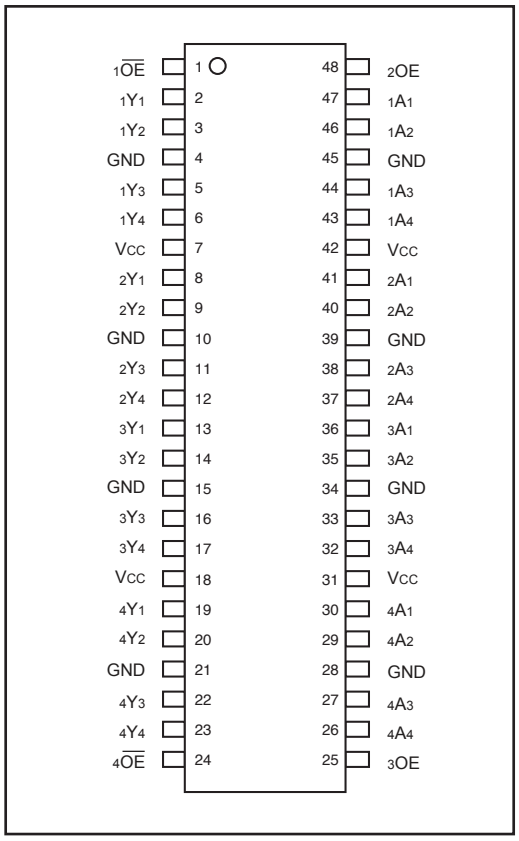
DESCRIPTION:

Potato Semiconductor's PO74G16241A is designed for world top performance using submicron CMOS technology to achieve 1.125GHz TTL /CMOS output frequency with less than 1.5ns propagation delay. This Octal bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation.

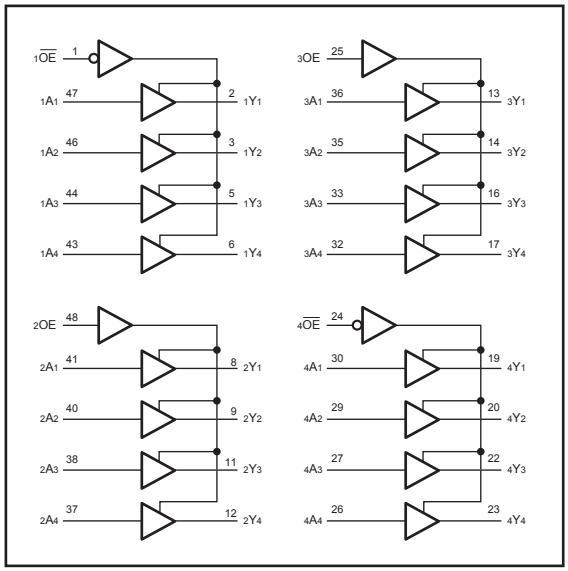
The PO74G16241A features independent line driver swith 3-state outputs. Each output is disabled when the associated output- enable input is high or low.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

Pin Configuration



Logic Block Diagram



Truth Table

Inputs		Outputs
$1\overline{OE}$, $4\overline{OE}$	1A, 4A	1Y, 4Y
L	H	H
L	L	L
H	X	Z

Inputs		Outputs
2OE, 3OE	2A, 3A	2Y, 3Y
H	H	H
H	L	L
L	X	Z

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Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:
stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=12mA	-	0.3	0.5	V
V_{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	5.5	V
V_{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I_{IH}	Input High current	Vcc = 3.6V and Vin = 5.5V	-	-	1	uA
I_{IL}	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-1	uA
V_{IK}	Clamp diode voltage	Vcc = Min. And I_{IN} = -18mA	-	-0.7	-1.2	V

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

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Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA
ΔI_{CC}	Power Supply Current per Input High	Vcc=Max, Vin= Vcc-0.6V	-	50	300	uA

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Capacitance

Parameters (1)	Description	Test Conditions	Typ	Unit
Cin	Input Capacitance	Vin = 0V	4	pF
Cout	Output Capacitance	Vout = 0V	6	pF

Notes:
1 This parameter is determined by device characterization but not production tested.

Switching Characteristics

Symbol	Description	Test Conditions (1)	Max	Unit
t_{PLH}	Propagation Delay A to Y	CL = 15pF	1.5	ns
t_{PHL}	Propagation Delay A to Y	CL = 15pF	1.5	ns
t_{PZH} or t_{PZL}	Output Enable Time	CL = 15pF	2.5	ns
t_{PHZ} or t_{PLZ}	Output Disable Time	CL = 15pF	2.5	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	ns
fmax	Input Frequency	CL = 50 pF	100	MHz
fmax	Input Frequency	CL =15pF	300	MHz
fmax	Input Frequency	CL = 5pF	750	MHz
fmax	Input Frequency	CL = 2pF	1125	MHz

Notes:
1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

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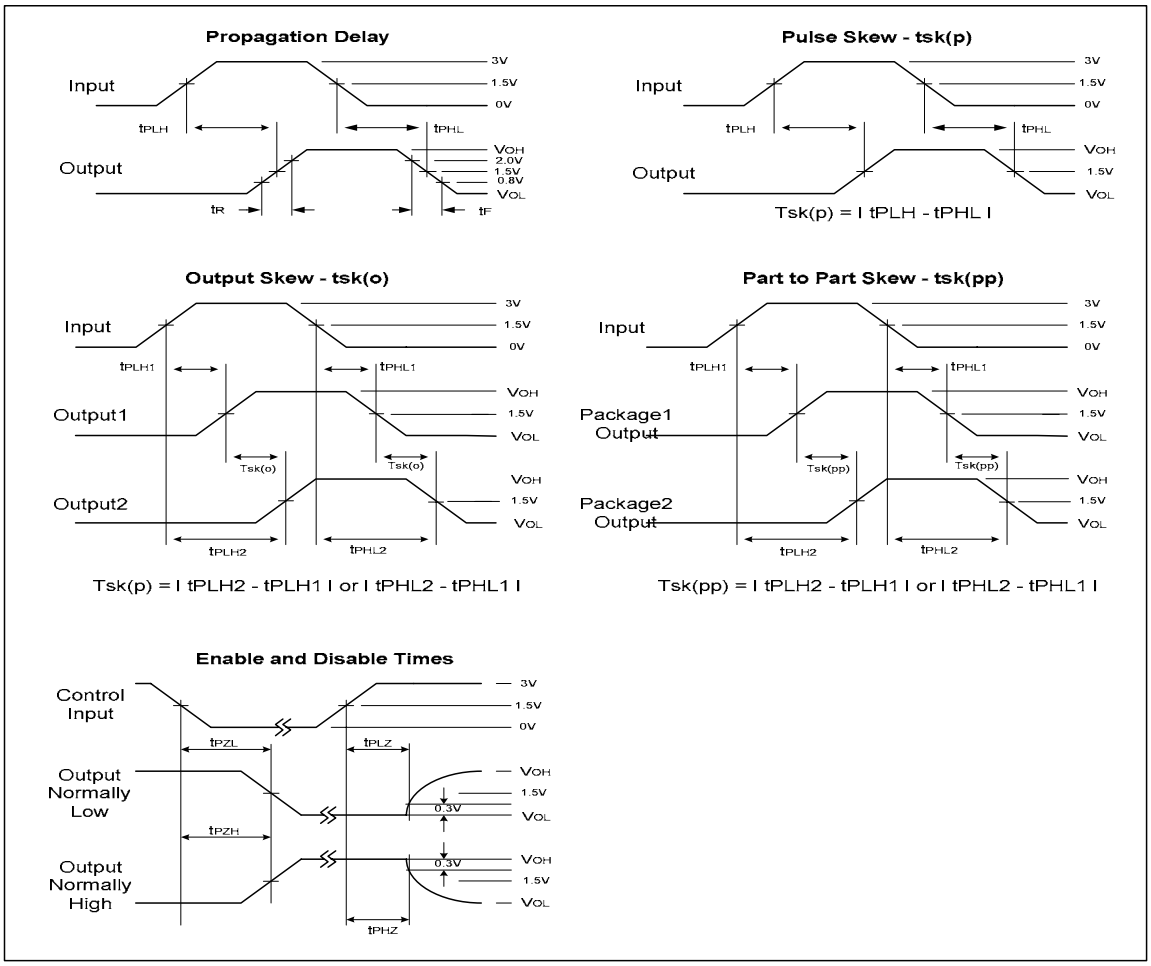
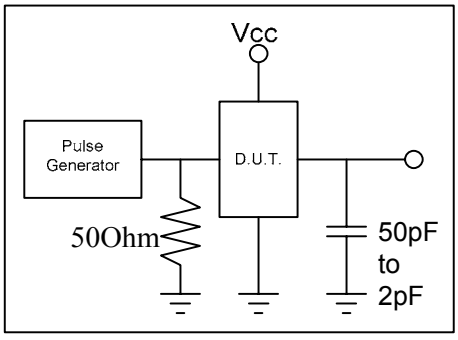
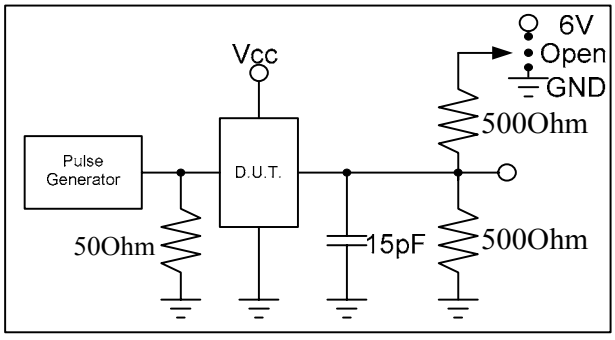
Test Waveforms

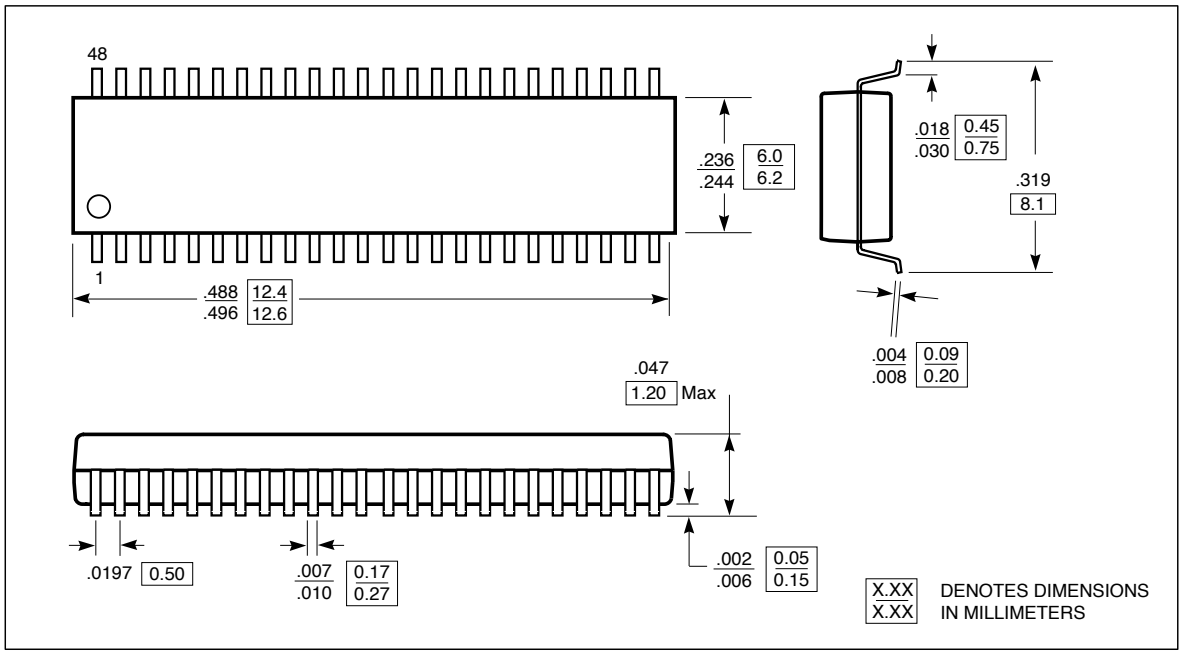


Test Circuit





Packaging Mechanical Drawing: 48 pin TSSOP



IC Ordering Information

Ordering Code	Package		Top-Marking	T_A
PO74G16241ASU for Tube	48pin TSSOP	Pb-free & Green	POTATO74G16241AS	-40°C to 85°C
PO74G16241ASR for Tape & Reel	48pin TSSOP	Pb-free & Green	POTATO74G16241AS	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER REEL	TAPE LEADER LENGTH	QTY PER TUBE
T	TSSOP 48	24	12	Top Left Corner	26 (12")	1500	43 (20")	39