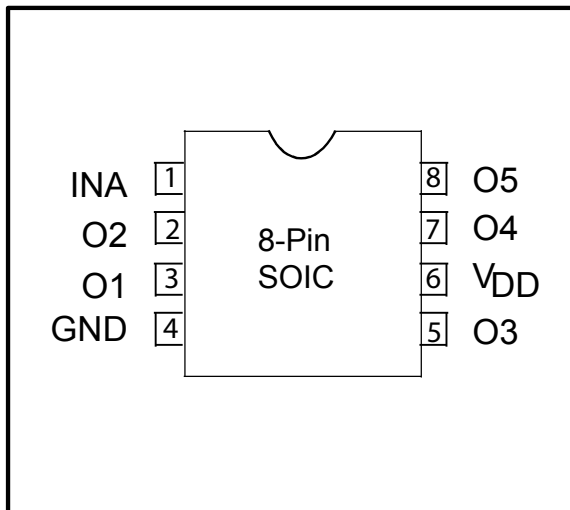
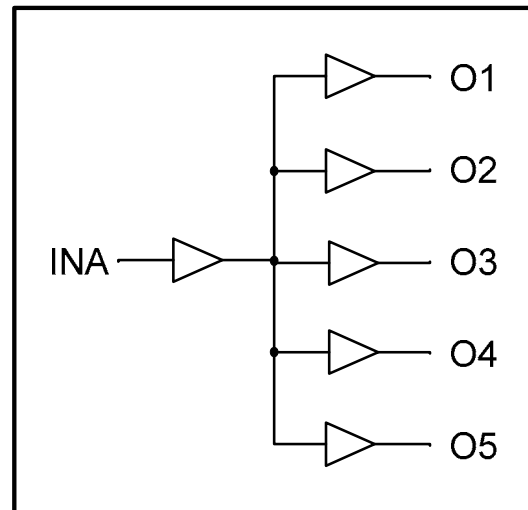


**750MHz TTL/CMOS Potato Chip**

FEATURES:	DESCRIPTION:
. Patented technology . Max input frequency > 1GHz . Operating frequency up to 750MHz with 2pf load . Operating frequency up to 600MHz with 5pf load . Operating frequency up to 300MHz with 15pf load . Operating frequency up to 125MHz with 50pf load . Very low output pin to pin skew < 80ps . Very low pulse skew < 130ps . VCC = 1.2V to 3.6V . Propagation delay < 1.5ns max with 15pf load . Low input capacitance: 3pf typical . 1:5 fanout . Available in 8pin 150mil wide SOIC package	Potato Semiconductor's PO74G2305A is designed for world top performance using submicron CMOS technology to achieve 750MHz TTL output frequency with less than 80ps output pin to pin skew. PO74G2305A is a 3.3V CMOS 1 input to 5 outputs Buffered driver to achieve 750MHz output frequency. Typical applications are clock and signal distribution. Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

Pin Configuration**Logic Block Diagram****Pin Description**

Pin Name	Description
INA	Input
O1 to O5	Outputs

**750MHz TTL/CMOS Potato Chip****Maximum Ratings**

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:

stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
VOH	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -12mA	2.4	3	-	V
VOL	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=12mA	-	0.3	0.5	V
VIH	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	Vcc	V
VIL	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
IHH	Input High current	Vcc = 3.6V and Vin = 5.5V	-	-	5	uA
IIL	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-5	uA
VIK	Clamp diode voltage	Vcc = Min. And IIN = -18mA	-	-0.7	-1.2	V

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

**750MHz TTL/CMOS Potato Chip****Power Supply Characteristics**

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
Iccq	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	50	uA
ΔIcc	Power Supply Current per Input High	Vcc=Max, Vin= Vcc-0.6V	-	50	300	uA

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Capacitance

Parameters (1)	Description	Test Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0V	3	4	pF
Cout	Output Capacitance	Vout = 0V	-	6	pF

Notes:

- 1 This parameter is determined by device characterization but not production tested.

Switching Characteristics

Symbol	Description	Test Conditions (1)	Max	Unit
tPLH	Propagation Delay A to Bn	CL = 15pF	1.5	ns
tPHL	Propagation Delay A to Bn	CL = 15pF	1.5	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	ns
tsk(p)	Pulse Skew (Same Package)	CL = 15pF, 125MHz	80	ps
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	0.13	ns
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz	0.4	ns
fmax	Input Frequency	CL = 50pF	125	MHz
fmax	Input Frequency	CL = 15pF	300	MHz
fmax	Input Frequency	CL = 5pF	600	MHz
fmax	Input Frequency	CL = 2pF	750	MHz

Notes:

1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

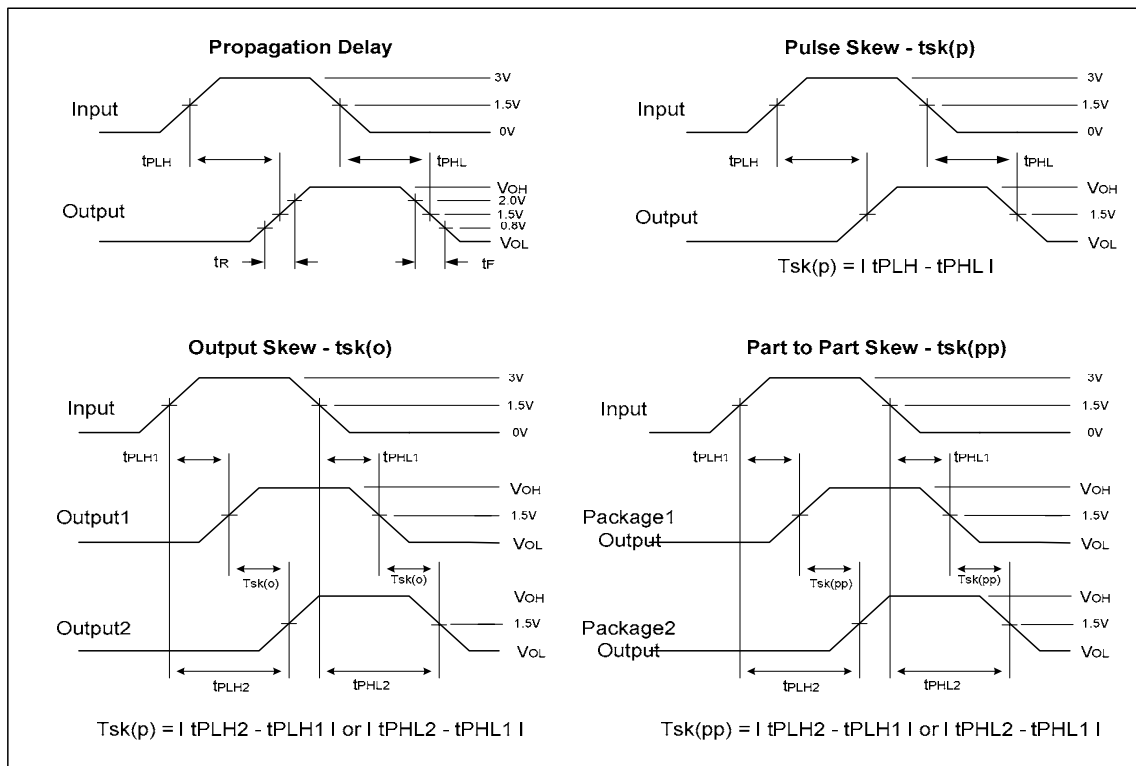


PO74G2305A

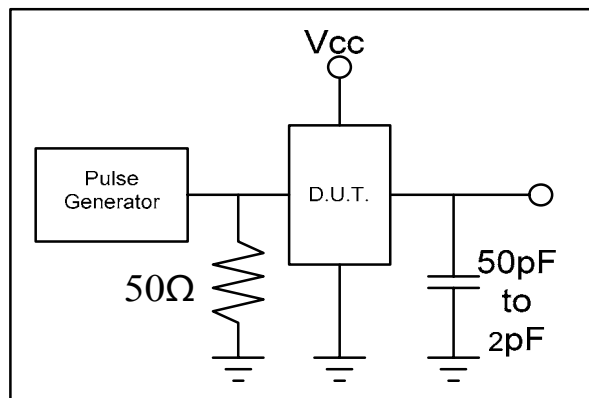
1.2V - 3.6V 1:5 CMOS Clock Buffered Driver

750MHz TTL/CMOS Potato Chip

Test Waveforms



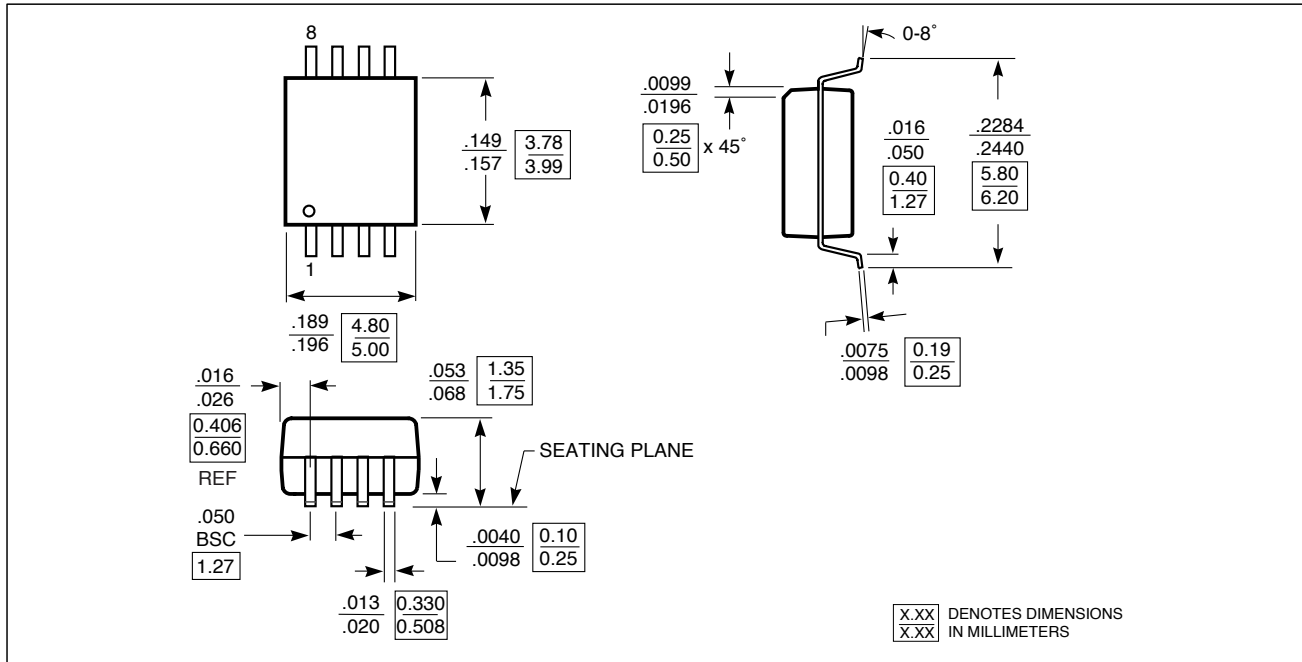
Test Circuit





750MHz TTL/CMOS Potato Chip

Packaging Mechanical Drawing: 8 pin SOIC



IC Ordering Information

Ordering Code	Package		Top-Marking	T _A
PO74G2305ASU for Tube	8-pin 150mil SOIC	Pb-free & Green	PO74G2305AS	-40°C to 85°C
PO74G2305ASR for Tape & Reel	8-pin 150mil SOIC	Pb-free & Green	PO74G2305AS	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	TAPE & REEL PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER TAPE	TAPE LEADER LENGTH	QTY PER TUBE
S	8-pin 150mil SOIC	16	8	Top Left Corner	39 (12")	3000	64 (20")	97