



PO74G2309A

1.2V - 3.6V 1:9 CMOS Clock Buffered Driver

700MHz TTL/CMOS Potato Chip

FEATURES:

- . Patented technology
- . Operating frequency up to 700MHz with 2pf load
- . Operating frequency up to 550MHz with 5pf load
- . Operating frequency up to 350MHz with 15pf load
- . Operating frequency up to 100MHz with 50pf load
- . Very low output pin to pin skew < 100ps
- . Very low pulse skew < 200ps
- . VCC = 1.2V to 3.6V
- . Propagation delay < 1.9ns max with 15pf load
- . Low input capacitance: 3pf typical
- . 1:9 fanout
- . Available in 16pin 150mil wide SOIC package
- . Available in 16pin 173mil wide TSSOP package

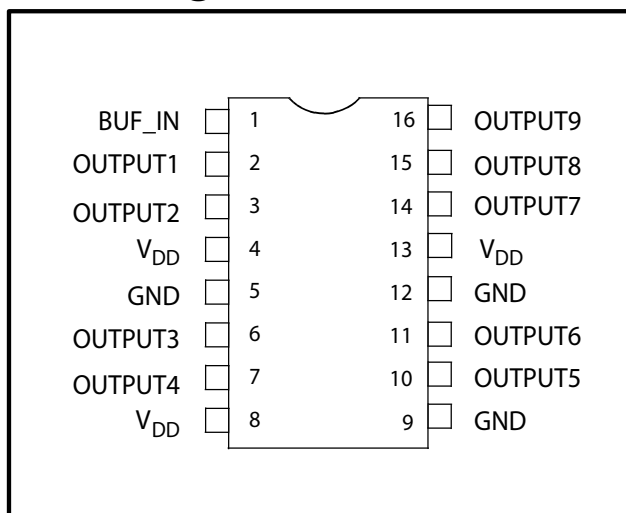
DESCRIPTION:

Potato Semiconductor's PO74G2309A is designed for world top performance using submicron CMOS technology to achieve 700MHz output frequency with less than 100ps output pin to pin skew.

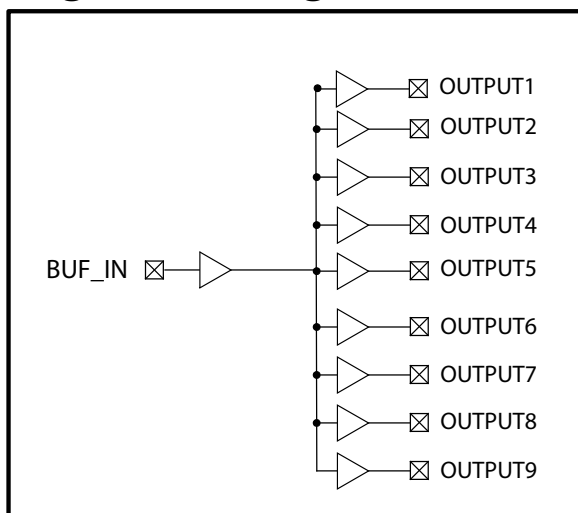
PO74G2309A is a 1.2V to 3.6V CMOS 1 input to 9 Output Buffered Driver to achieve 700MHz output frequency. Typical applications are clock and signal distribution.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

Pin Configuration



Logic Block Diagram



Pin Description

Pin Name	Description
BUF_IN	Input
OUTPUT 1 to OUTPUT 9	Outputs

**700MHz TTL/CMOS Potato Chip****Maximum Ratings**

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:

stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
VOH	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -12mA	2.4	3	-	V
VOL	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=12mA	-	0.3	0.5	V
VIH	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	5.5	V
VIL	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
IIH	Input High current	Vcc = 3.6V and Vin = 5.5V	-	-	1	uA
IIL	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-1	uA
VIK	Clamp diode voltage	Vcc = Min. And IIN = -18mA	-	-0.7	-1.2	V

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc - 0.6V at rated current

**700MHz TTL/CMOS Potato Chip****Power Supply Characteristics**

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
Iccq	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	60	uA

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Capacitance

Parameters (1)	Description	Test Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0V	3	4	pF
Cout	Output Capacitance	Vout = 0V	-	6	pF

Notes:

- 1 This parameter is determined by device characterization but not production tested.

Switching Characteristics

Symbol	Description	Test Conditions (1)	Max	Unit
tPLH	Propagation Delay Buf_in to Output1 to Output9	CL = 15pF	1.9	ns
tPHL	Propagation Delay Buf_in to Output1 to Output9	CL = 15pF	1.9	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	ns
tsk(p)	Pulse Skew (Same Package)	CL = 15pF, 125MHz	200	ps
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	100	ps
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz	400	ps
fmax	Input Frequency	CL = 50pF	100	MHz
fmax	Input Frequency	CL = 15pF	350	MHz
fmax	Input Frequency	CL = 5pF	550	MHz
fmax	Input Frequency	CL = 2pF	700	MHz

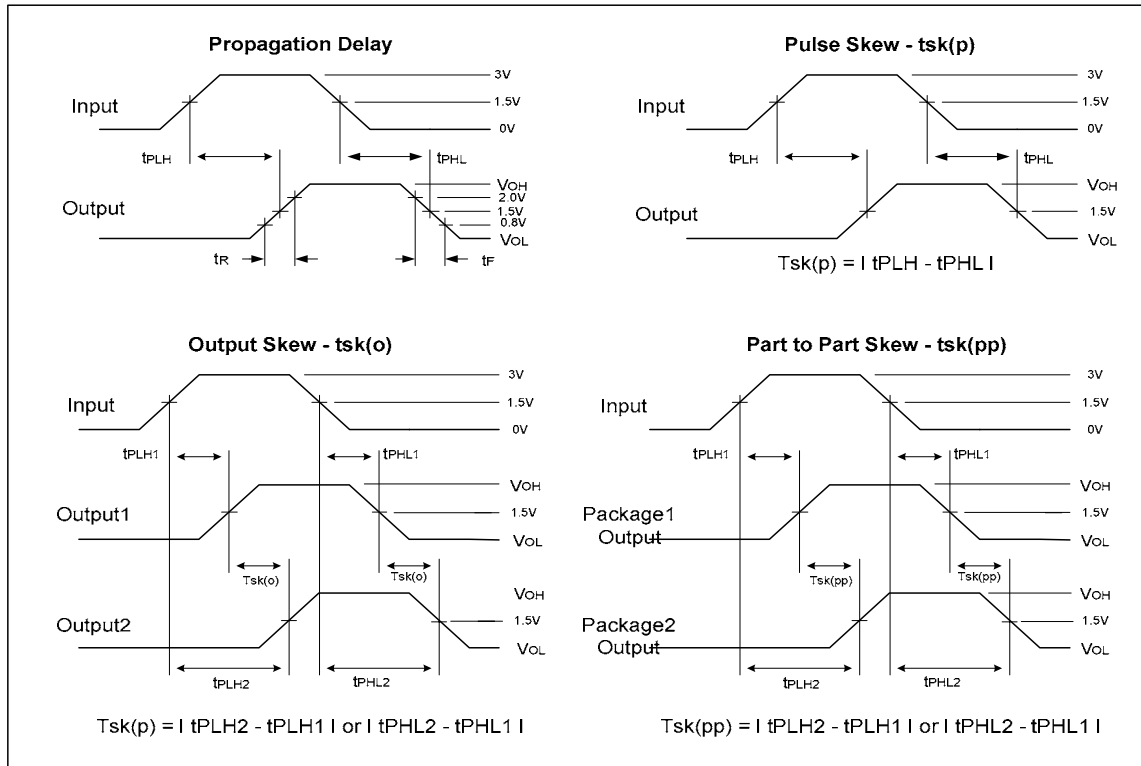
Notes:

1. See test circuits and waveforms.
2. tPLH, tPHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

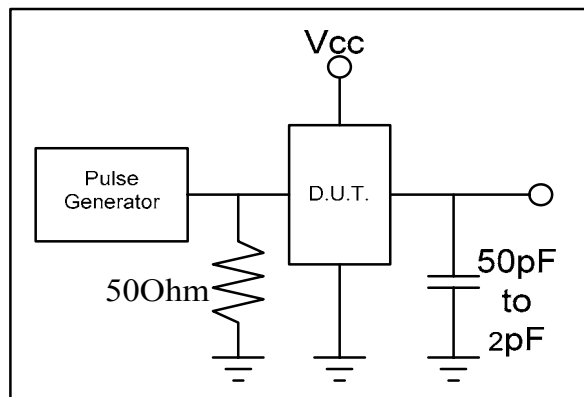


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Test Waveforms



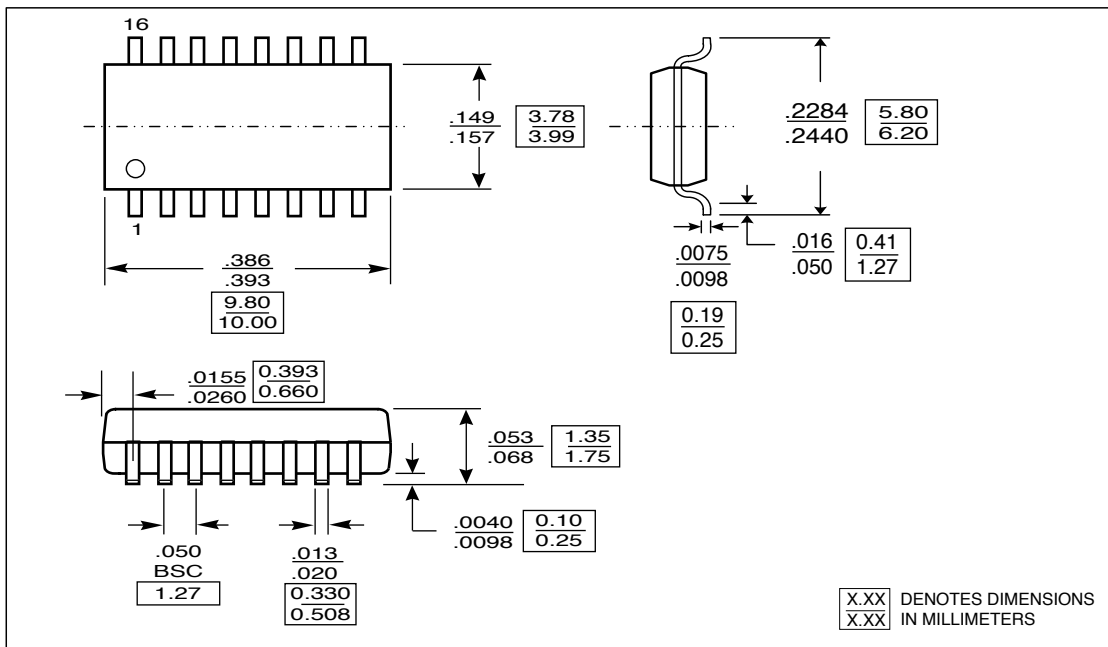
Test Circuit



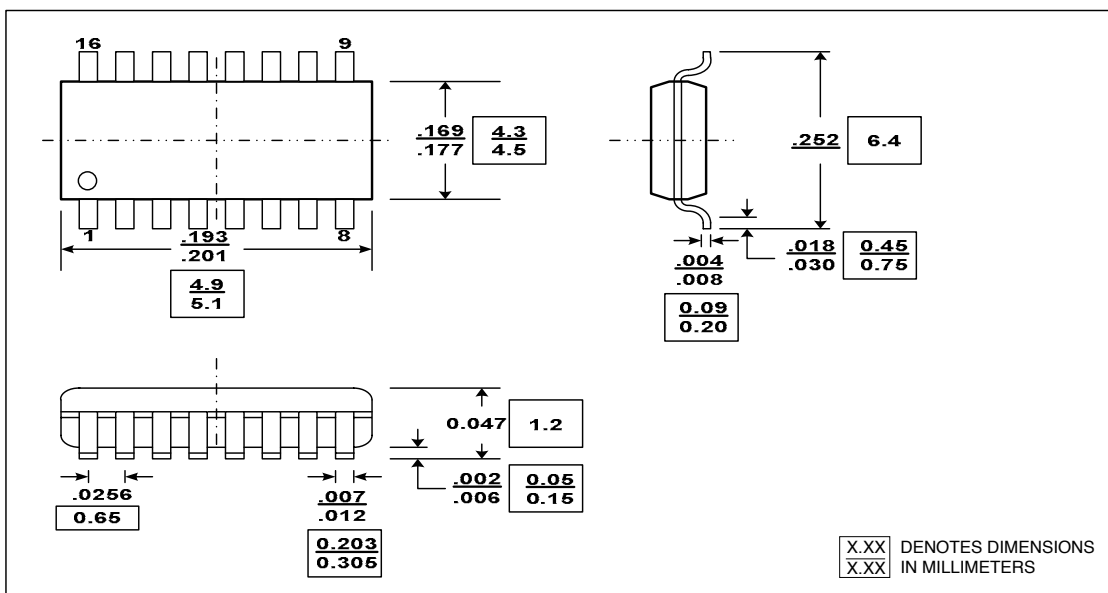


700MHz TTL/CMOS Potato Chip

Packaging Mechanical Drawing: 16 pin SOIC



Packaging Mechanical Drawing: 16 pin TSSOP



**700MHz TTL/CMOS Potato Chip****IC Ordering Information**

Ordering Code	Package		Top-Marking	T _A
PO49FCT2309ASU for Tube	16-pin 150mil QSOP	Pb-free & Green	PO49FCT2309AQ	-40°C to 85°C
PO49FCT2309ASR for Tape & Reel	16-pin 150mil QSOP	Pb-free & Green	PO49FCT2309AQ	-40°C to 85°C
PO49FCT2309ATU for Tube	16-pin 173mil TSSOP	Pb-free & Green	PO49FCT2309AT	-40°C to 85°C
PO49FCT2309ATR for Tape & Reel	16-pin 173mil TSSOP	Pb-free & Green	PO49FCT2309AT	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	TAPE & REEL PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER TAPE	TAPE LEADER LENGTH	QTY PER TUBE
S	16pin 150mil SOIC	12	8	Top Left Corner	39 (12")	3000	64 (20")	48
T	16pin 173mil TSSOP	12	8	Top Left Corner	39 (12")	3000	64 (20")	96