

512Kx9 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- Performance range:

	t _{RAC}	t _{CAC}	t _{RC}
KM49C512- 7	70ns	20ns	130ns
KM49C512- 8	80ns	20ns	150ns
KM49C512-10	100ns	25ns	180ns

- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Dual +5V \pm 10% power supply
- 1024 cycles/16ms refresh
- JEDEC Standard pinout
- Available in Plastic SOJ

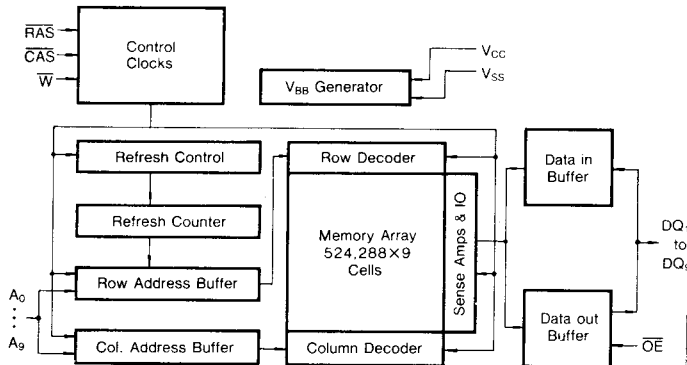
GENERAL DESCRIPTION

The Samsung KM49C512 is a CMOS high speed 524,288 bit \times 9 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM49C512 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

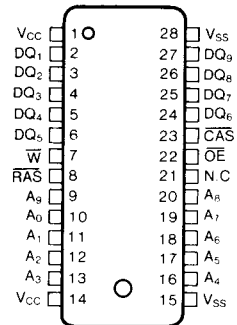
The KM49C512 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- KM49C512J



Pin Name	Pin Function
A ₀ -A ₉	Address Inputs
DQ ₁₋₉	Data In/Out
V _{SS}	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
V _{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	700	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} +1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Operating Current* (RAS and CAS Cycling @ t _{RC} =min)	KM49C512- 7	I _{CC1}	110	mA
	KM49C512- 8		95	mA
	KM49C512-10		80	mA
Standby Current (RAS=CAS=V _{IH})	I _{CC2}		2	mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @ t _{RC} =min)	KM49C512- 7	I _{CC3}	110	mA
	KM49C512- 8		95	mA
	KM49C512-10		80	mA
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @ t _{PC} =min.)	KM49C512- 7	I _{CC4}	85	mA
	KM49C512- 8		75	mA
	KM49C512-10		65	mA
Standby Current (RAS=CAS=V _{CC} -0.2V)	I _{CC5}		1	mA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @ t _{RC} =min)	KM49C512- 7	I _{CC6}	110	mA
	KM49C512- 8		95	mA
	KM49C512-10		80	mA
Standby Current (RAS=V _{IH} , CAS=V _{IL} Dout=Enable)	I _{CC7}		5	mA
Input Leakage Current (Any input 0≤V _{IN} ≤6.5V, all other pins not under test=0 volts.)	I _{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤5.5V)	I _{OL}	-10	10	μA
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	—	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while RAS=V_{IL}. I_{CC4}, Address can be changed maximum once while CAS=V_{IH}.



CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ -A ₉)	C _{IN1}	—	6	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$)	C _{IN2}	—	7	pF
Output Capacitance (DQ ₁ -DQ ₉)	C _{DQ}	—	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC}=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	KM49C512-7		KM49C512-8		KM49C512-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	130		150		180		ns	
Read-modify-write cycle time	t _{RWC}	185		205		245		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{\text{CAS}}$	t _{CAC}		20		20		25	ns	3,4,5
Access time from column address	t _{AA}		35		40		45	ns	3,11
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t _{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t _T	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	t _{RP}	50		60		70		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	20		20		25		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	70		80		100		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	50	20	60	25	75	ns	4
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	35	15	40	20	50	ns	11
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5		5		10		ns	
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	10		10		15		ns	
Column address set-up time	t _{ASC}	0		0		0		ns	
Column address hold time	t _{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	t _{AR}	55		60		75		ns	6
Column Address to $\overline{\text{RAS}}$ lead time	t _{RAL}	35		40		50		ns	
Read command set-up time	t _{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	9
Write command hold time	t _{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t _{WCR}	55		60		75		ns	6
Write command pulse width	t _{WP}	10		10		20		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWI}	20		20		25		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	20		20		25		ns	
Data-in set-up time	t _{DS}	0		0		0		ns	10
Data-in hold time	t _{DH}	15		15		20		ns	10

AC CHARACTERISTICS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$. See notes 1,2)

Parameter	Symbol	KM49C512-7		KM49C512-8		KM49C512-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time referenced to $\overline{\text{RAS}}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t_{CWD}	50		50		60		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t_{RWD}	100		110		135		ns	8
Column address to $\overline{\text{W}}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{\text{CAS}}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	100		105		120		ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{\text{CAS}}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	t_{ROH}	20		20		20		ns	
$\overline{\text{OE}}$ access time	t_{OEA}		20		20		25	ns	
$\overline{\text{OE}}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	$t_{O EZ}$	0	20	0	20	0	25	ns	
$\overline{\text{OE}}$ command hold time	$t_{OE H}$	20		20		25		ns	

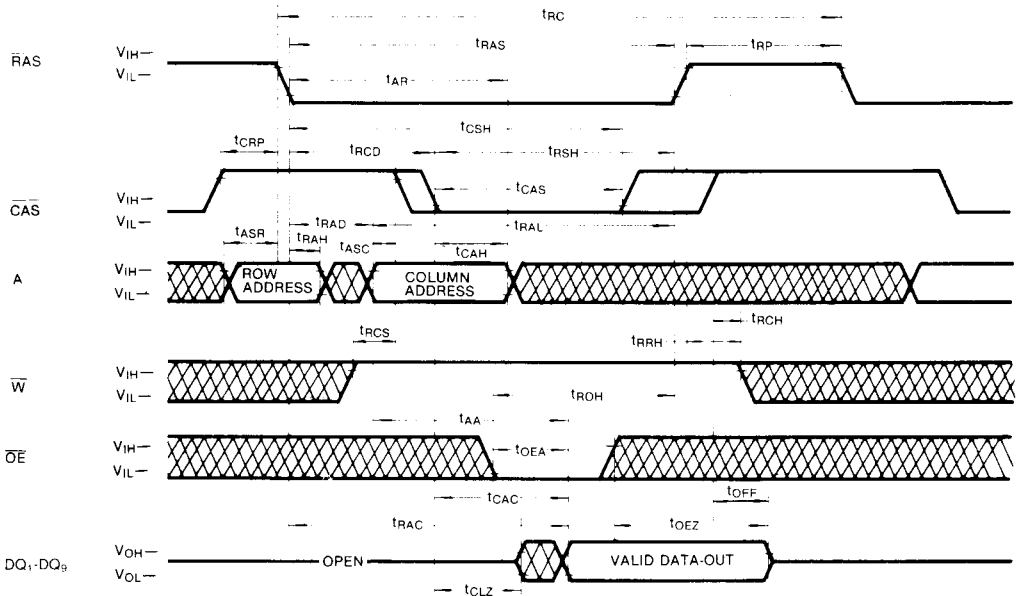
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NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}}(\text{max})$.
7. $t_{\text{OFF}}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL} .
8. t_{WCS} , t_{RWD} , and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .

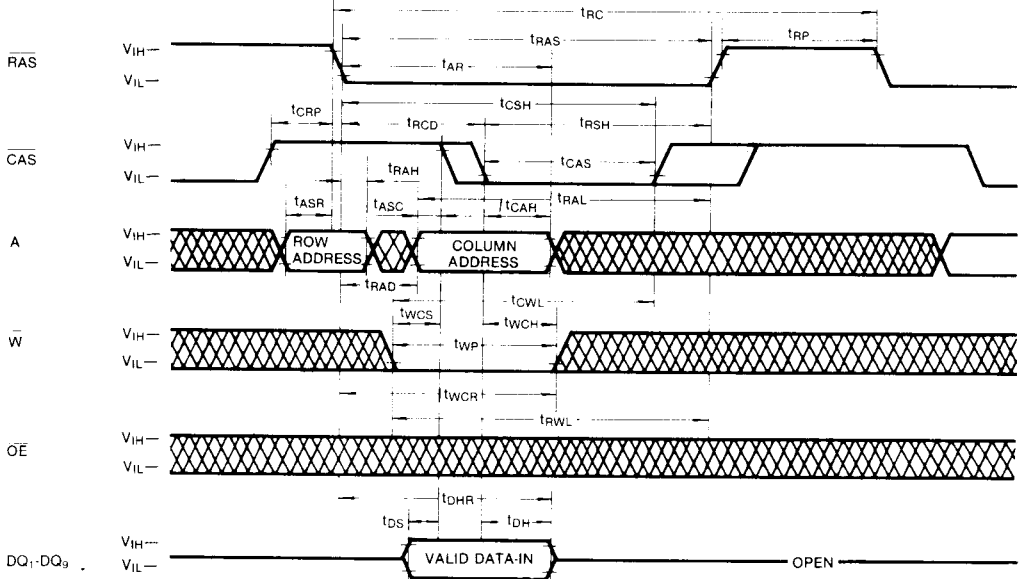
TIMING DIAGRAMS

READ CYCLE

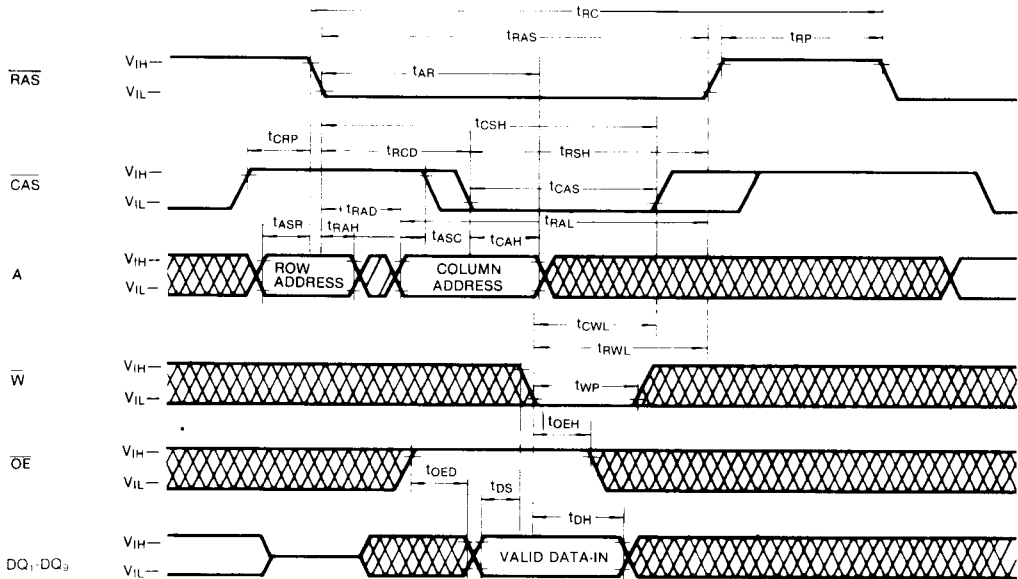


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



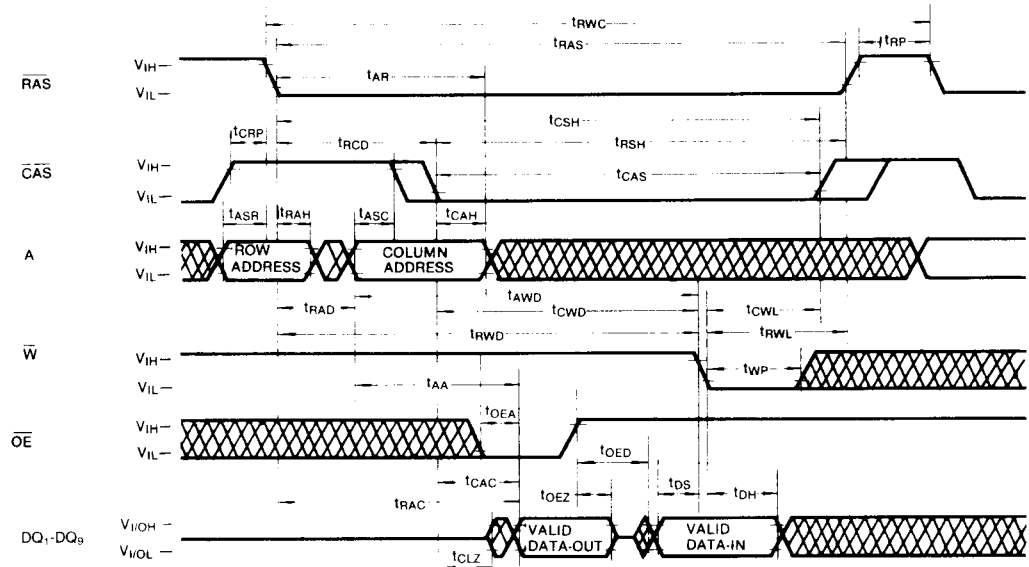
WRITE CYCLE (OE CONTROLLED WRITE)



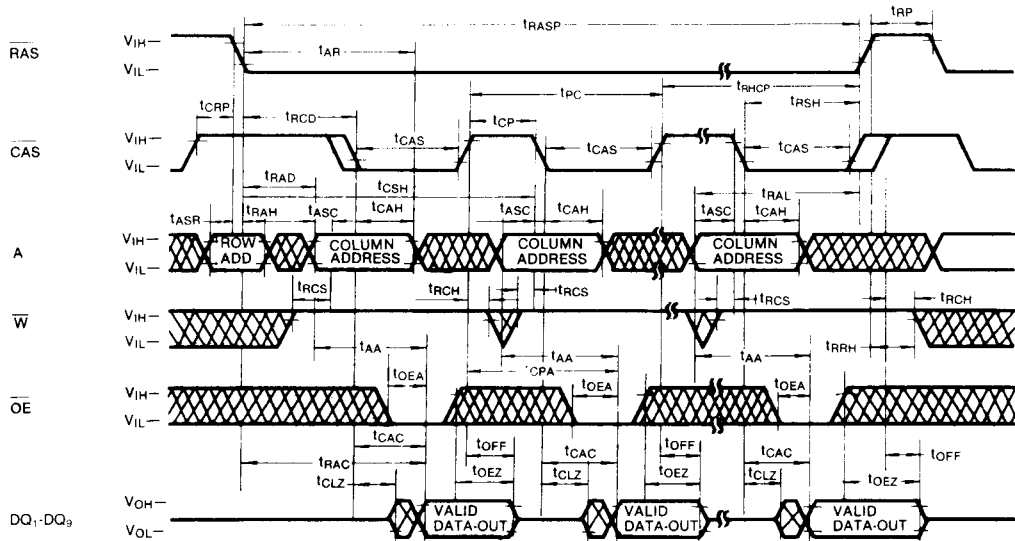
 DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

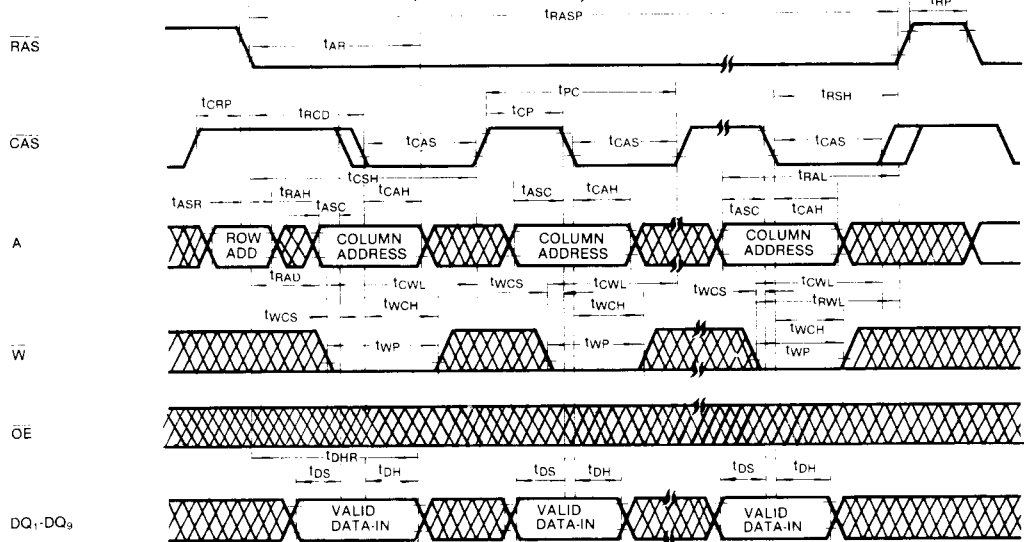


DON'T CARE

KM49C512

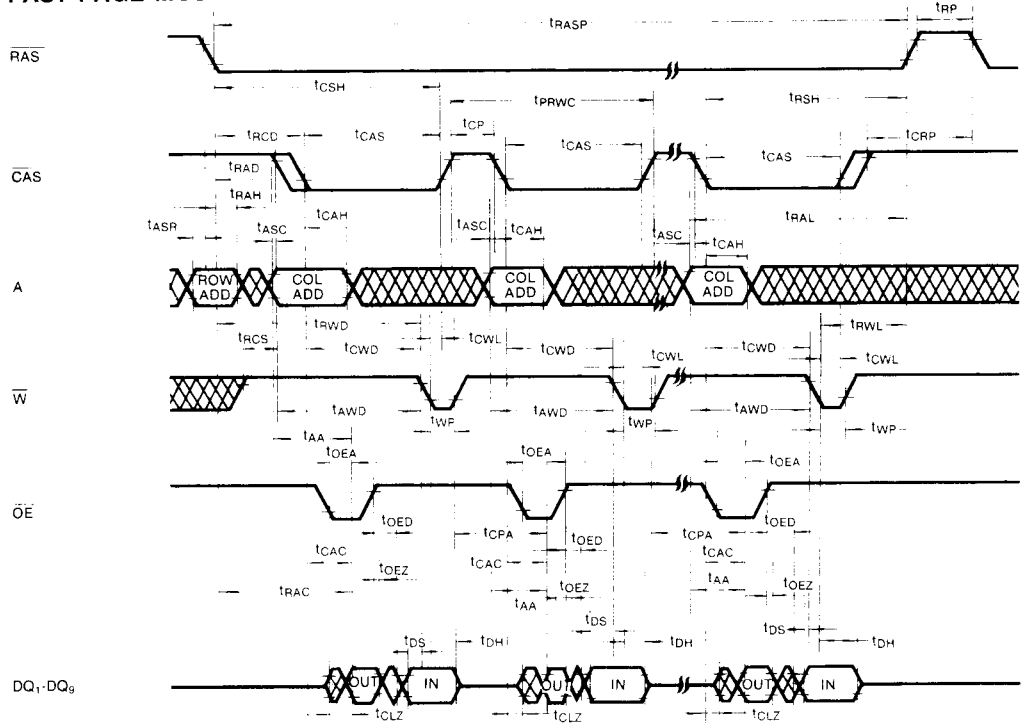
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



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FAST PAGE MODE READ-MODIFY-WRITE

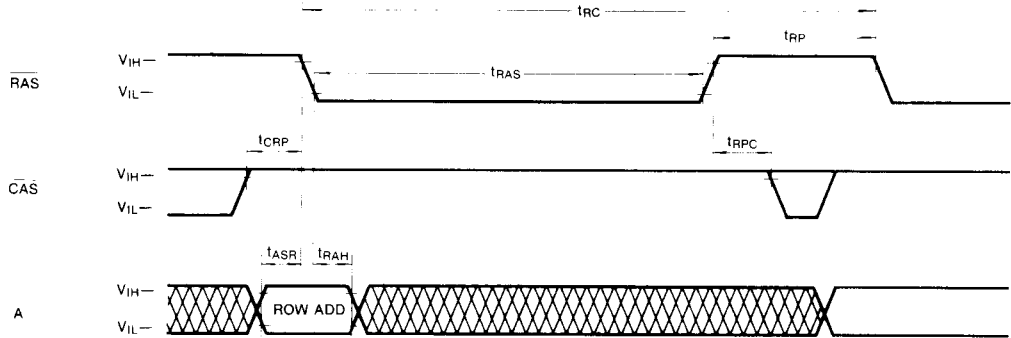


DON'T CARE

TIMING DIAGRAMS (Continued)

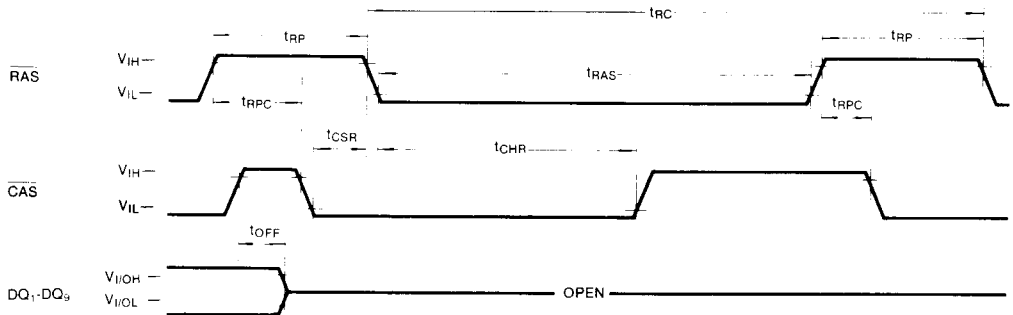
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , \bar{OE} = Don't care



CAS-BEFORE-RAS REFRESH CYCLE

NOTE: $\bar{W}=V_{IH}$, \bar{OE} , A=Don't Care

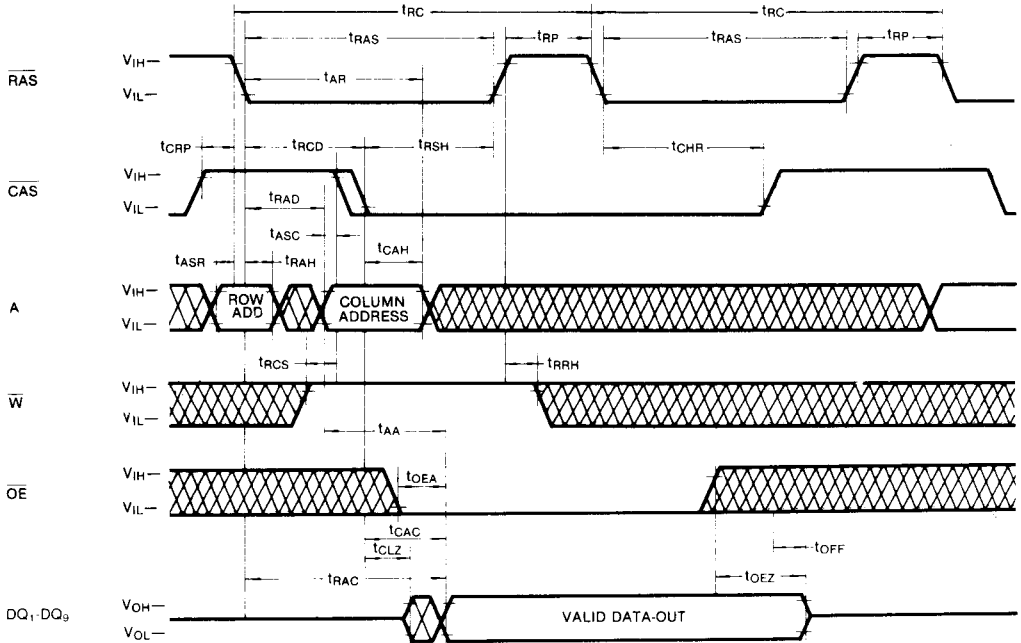


 DON'T CARE

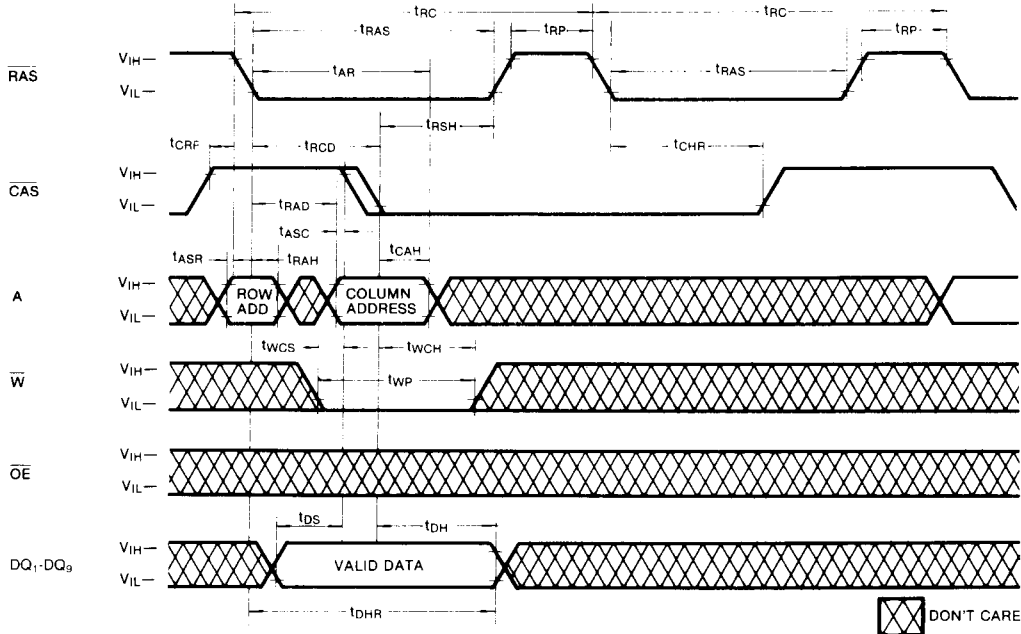
KM49C512

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

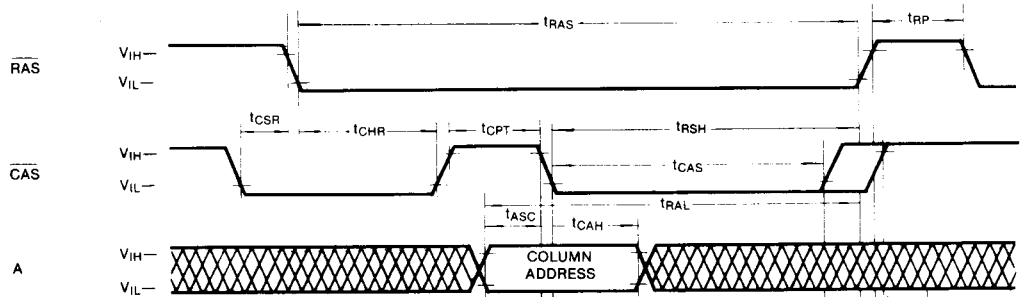


HIDDEN REFRESH CYCLE (WRITE)

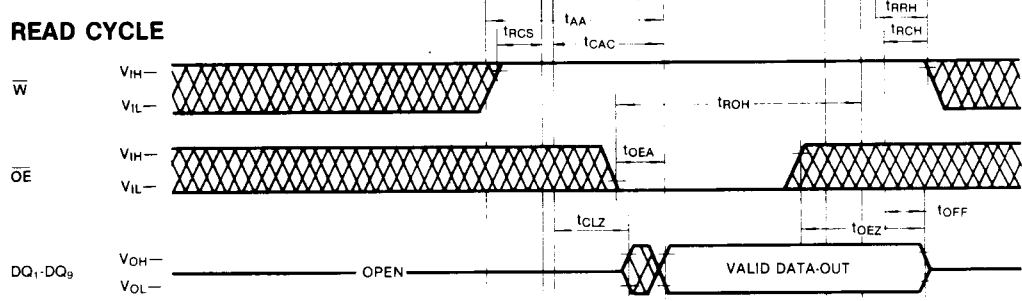


TIMING DIAGRAMS (Continued)

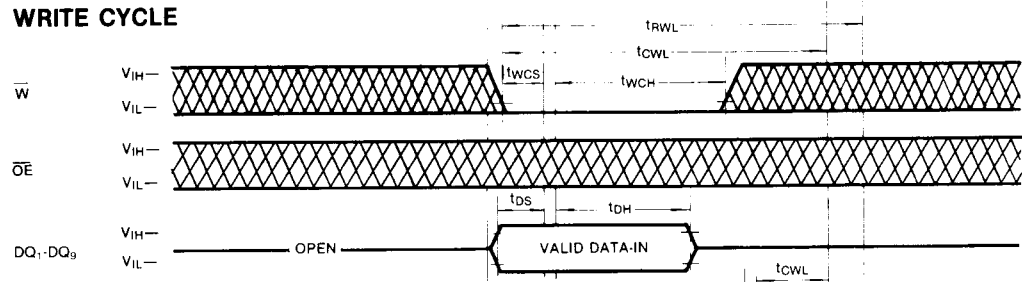
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



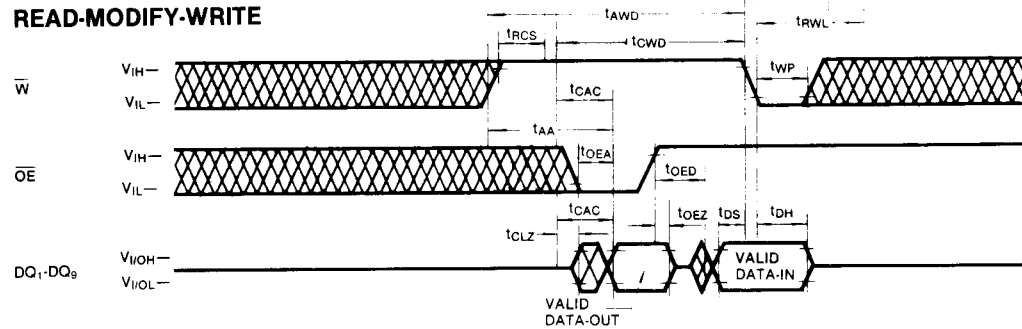
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



 DON'T CARE

DEVICE OPERATION

Device Operation

The KM49C512 contains 4,718,592 memory locations arranged in 9 groups of 524,288×1 bit each. Twenty-address bits are required to address a particular memory location. Since the KM49C512 has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the column address strobe (\overline{CAS}) and the valid row and column address inputs.

Operation of the KM49C512 begins by strobing in a valid row address with \overline{RAS} while \overline{CAS} remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by \overline{CAS} . This is the beginning of any KM49C512 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{CAS} have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the \overline{RAS} precharge time (t_{RP}) requirement.

\overline{RAS} and \overline{CAS} Timing

The minimum \overline{RAS} and \overline{CAS} pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CAS} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM49C512 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input (\overline{W}) high during a $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of \overline{RAS} . Additionally the access time also depends on the falling edge of \overline{CAS} and on the valid column address transition. If \overline{CAS} transitions to a low before $t_{RCD(max)}$ then the access time to valid data is specified by $t_{RAC(min)}$. However, if \overline{CAS} transitions low after $t_{RCD(max)}$ or if the column address becomes valid after $t_{RAD(max)}$, access is specified by t_{CAC} or t_{AA} . In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAD(max)}$.

Write

The KM49C512 can perform early write, late write and

read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} , \overline{OE} , \overline{CAS} . In any type of write cycle, Data-in must be valid at or before the falling edge of \overline{W} or \overline{CAS} , whichever is later.

Early Write: An early write cycle is performed by bringing \overline{W} low before \overline{CAS} . The 9-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the \overline{OE} input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing \overline{W} low after \overline{CAS} and meeting the data sheet read-modify-write timing requirements. The \overline{OE} input must be low during the time defined by t_{OE} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the \overline{OE} timing requirements prevents bus contention on the KM49C512 DQ pins.

Data Output

The KM49C512 has a three-state output buffers which are controlled by \overline{CAS} and \overline{OE} . Whenever either \overline{CAS} or \overline{OE} is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of \overline{CAS} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new \overline{RAS} cycle occurs (as in hidden refresh). Each of the KM49C512 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, \overline{RAS} -only Refresh, Fast Page Mode Write, \overline{CAS} -Before- \overline{RAS} Refresh, \overline{OE} controlled write, \overline{CAS} -only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

Refresh

The data in the KM49C512 is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will af-

DEVICE OPERATION (Continued)

fect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) of within 16ms. There are several ways to accomplish this:

\overline{RAS} -Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with \overline{RAS} while \overline{CAS} remains high. This cycle must be repeated for each of the 1024 row address (A0-A9).

\overline{CAS} -before- \overline{RAS} Refresh: The KM49C512 has \overline{CAS} -before- \overline{RAS} on-chip refresh capability that eliminates the need for external refresh addresses. If either \overline{CAS} input is held low for the specified set up time (t_{CSR}) before \overline{RAS} transitions low, the onchip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next \overline{CAS} -before- \overline{RAS} refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either input active time and cycling \overline{RAS} . The hidden refresh cycle is actually a \overline{CAS} -before- \overline{RAS} refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM49C512 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform

refresh in this manner but in general \overline{RAS} -only or \overline{CAS} -before- \overline{RAS} refresh is the preferred method.

Fast Page Mode

The KM49C512 has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while \overline{RAS} is held low to maintain the row address, \overline{CAS} is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

 \overline{CAS} -before- \overline{RAS} Refresh Counter test cycle

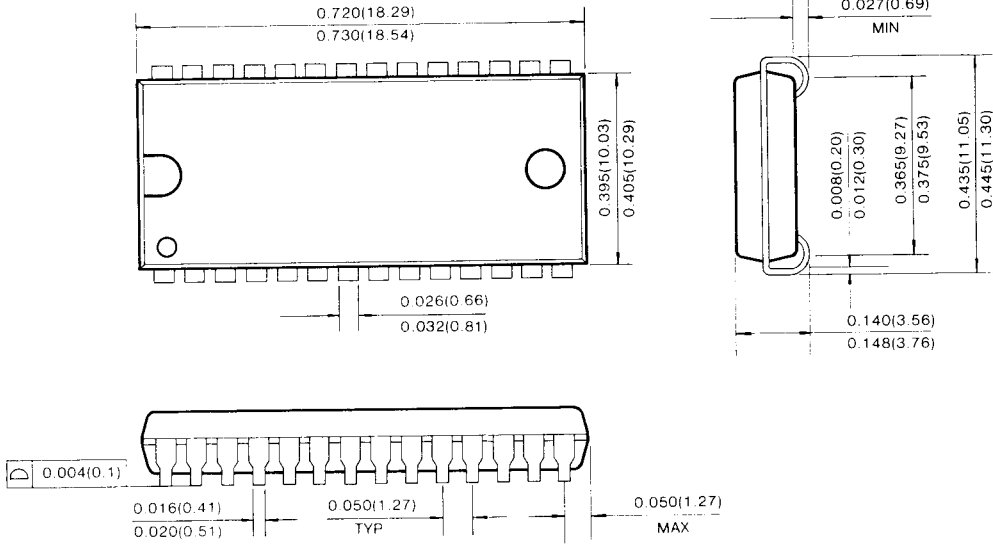
A special timing sequence using the \overline{CAS} -before- \overline{RAS} counter test cycle provides a convenient method of verifying the functionality of the \overline{CAS} -before- \overline{RAS} refresh activated circuitry. The cycle begins as a \overline{CAS} -before- \overline{RAS} refresh operation. Then, if \overline{CAS} is asserted high and then low again while \overline{RAS} is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A9 are supplied by on chip refresh counter.

Power-Up

If $\overline{RAS}=V_{SS}$ during power-up, the KM49C512 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that \overline{RAS} and \overline{CAS} track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize power-up current.

PACKAGE DIMENSION
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



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