

Document Title

32Kx8 bit Low Power CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	October 09, 2002	Preliminary
1.0	Finalized - Changed Icc from 10mA to 5mA - Changed Icc1 from 8mA to 7mA - Changed Icc2 from 35mA to 25mA - Changed Isb from 3mA to 0.4mA - Changed IdR for K6X0808C1D-F 15μA to 10μA - Changed IdR for K6X0808C1D-Q 25μA to 20μA - Errata correction	December 16, 2003	Final

The attached datasheets are provided by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserves the right to change the specifications and products. SAMSUNG Electronics will answer to your questions. If you have any questions, please contact the SAMSUNG branch offices.

32Kx8 bit Low Power full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 32K x 8
- Power Supply Voltage: 4.5–5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 28-DIP-600B, 28-SOP-450,
28-TSOP1-0813.4F/R

GENERAL DESCRIPTION

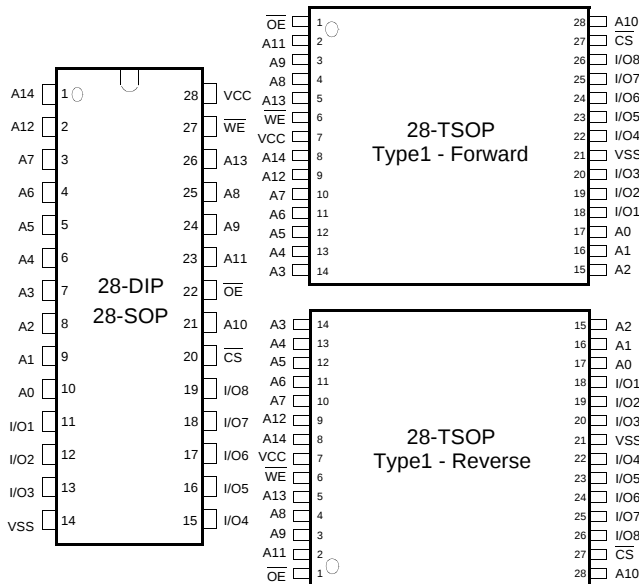
The K6X0808C1D families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{sb1} , Max)	Operating (I _{cc2} , Max)	
K6X0808C1D-F	Industrial(-40~85°C)	4.5–5.5V	55 ¹⁾ /70ns	15μA	25mA	28-DIP-600B, 28-SOP-450, 28-TSOP1-0813.4F/R
K6X0808C1D-Q	Automotive(-40~125°C)			25μA		28-SOP-450, 28-TSOP1-0813.4F

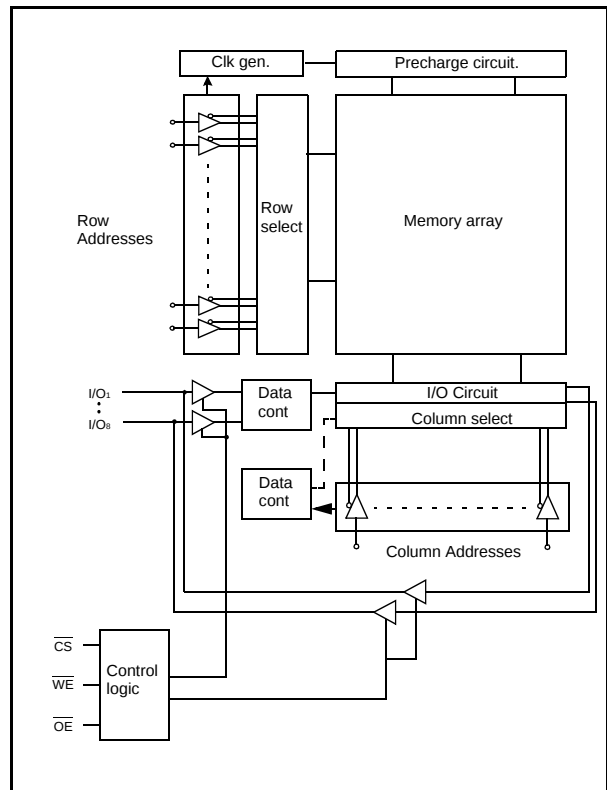
1. The parameters are tested with 50pF test load

PIN DESCRIPTION



Pin Name	Function	Pin Name	Function
$\overline{CS}$	Chip Select Input	I/O ₁ –I/O ₈	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
A ₀ –A ₁₄	Address Inputs	NC	No connect

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

PRODUCT LIST

Industrial Temp. Products(-40~85°C)		Automotive Temp. Products(-40~125°C)	
Part Name	Function	Part Name	Function
K6X0808C1D-DF55 K6X0808C1D-DF70 K6X0808C1D-GF55 K6X0808C1D-GF70 K6X0808C1D-TF55 K6X0808C1D-TF70 K6X0808C1D-RF55 K6X0808C1D-RF70	28-DIP, 55ns, LL Pwr 28-DIP, 70ns, LL Pwr 28-SOP, 55ns, LL Pwr 28-SOP, 70ns, LL Pwr 28-TSOP-F, 55ns, LL Pwr 28-TSOP-F, 70ns, LL Pwr 28-TSOP-R, 55ns, LL Pwr 28-TSOP-R, 70ns, LL Pwr	K6X0808C1D-GQ55 K6X0808C1D-GQ70 K6X0808C1D-TQ55 K6X0808C1D-TQ70	28-SOP, 55ns, L Pwr 28-SOP, 70ns, L Pwr 28-TSOP-F, 55ns, L Pwr 28-TSOP-F, 70ns, L Pwr

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5V(Max. 7.0V)	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to 7.0	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	-40 to 85	°C	K6X0808C1D-F
		-40 to 125	°C	K6X0808C1D-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.5 ²⁾	V
Input low voltage	V _{IL}	-0.5 ³⁾	-	0.8	V

Note:

1. Industrial Product: T_A=-40 to 85°C, Otherwise specified
Automotive Product: T_A=-40 to 125°C, Otherwise specified
2. Overshoot: V_{CC}+3.0V in case of pulse width≤30ns.
3. Undershoot: -3.0V in case of pulse width≤30ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , Read	-	-	5	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS} \leq 0.2V$, V _{IN} ≤0.2V _{IN} ≥V _{CC} -0.2V	-	-	7	mA
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL}	-	-	25	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}=V_{IH}$, Other inputs=V _{IH} or V _{IL}	-	-	0.4	mA
Standby Current (CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, Other inputs=0~V _{CC}				
		K6X0808C1D-F	-	-	15	μA
		K6X0808C1D-Q	-	-	25	μA

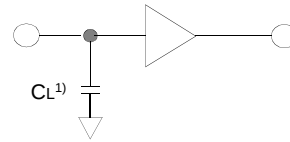
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.8 to 2.4V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (See right): $C_L=100\text{pF}+1\text{TTL}$ $C_L=50\text{pF}+1\text{TTL}$ 

1. Including scope and jig capacitance

AC CHARACTERISTICS ($V_{CC}=4.5\sim 5.5\text{V}$, Commercial product: $T_A=0$ to 70°C , Industrial product: $T_A=-40$ to 85°C)

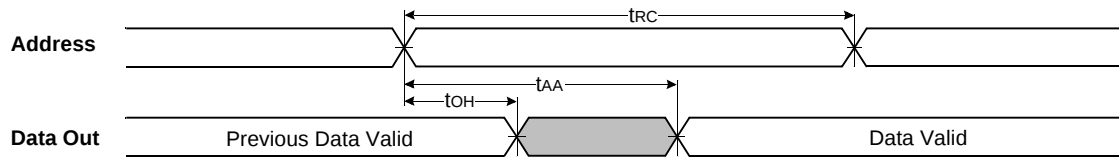
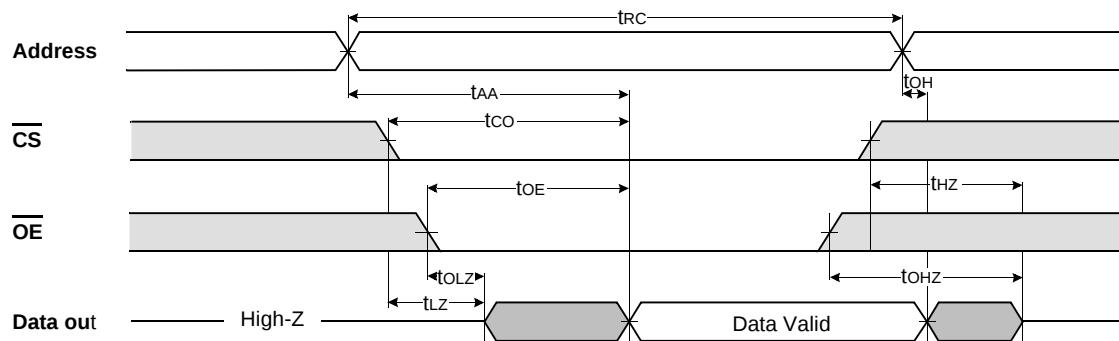
Parameter List		Symbol	Speed Bins				Units
			55 ¹⁾ ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	55	-	70	-	ns
	Address access time	t _{AA}	-	55	-	70	ns
	Chip select to output	t _{CO}	-	55	-	70	ns
	Output enable to valid output	t _{OE}	-	25	-	35	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	20	0	30	ns
	Output disable to high-Z output	t _{OHZ}	0	20	0	30	ns
	Output hold from address change	t _{OH}	10	-	10	-	ns
Write	Write cycle time	t _{WC}	55	-	70	-	ns
	Chip select to end of write	t _{CW}	45	-	60	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	45	-	60	-	ns
	Write pulse width	t _{WP}	40	-	50	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	20	0	25	ns
	Data to write time overlap	t _{DW}	25	-	30	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns

1. The parameter is tested with 50pF test load.

DATA RETENTION CHARACTERISTICS

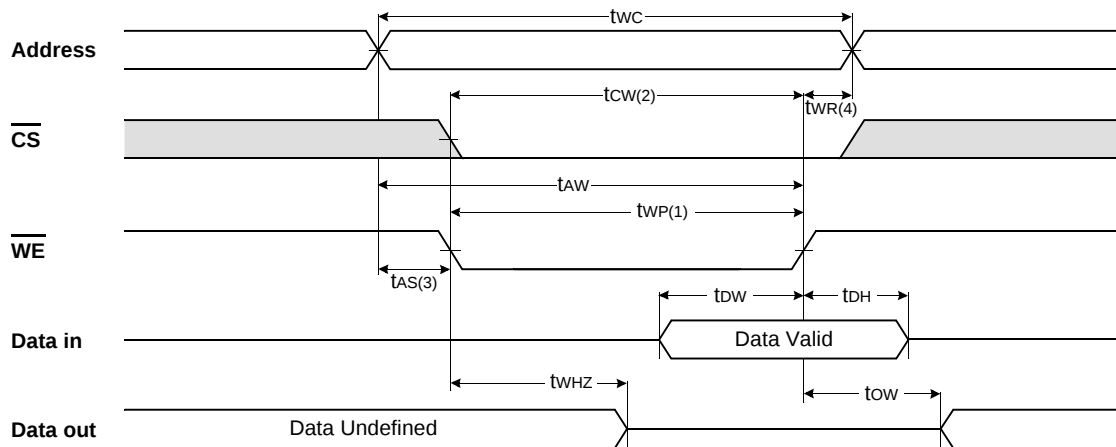
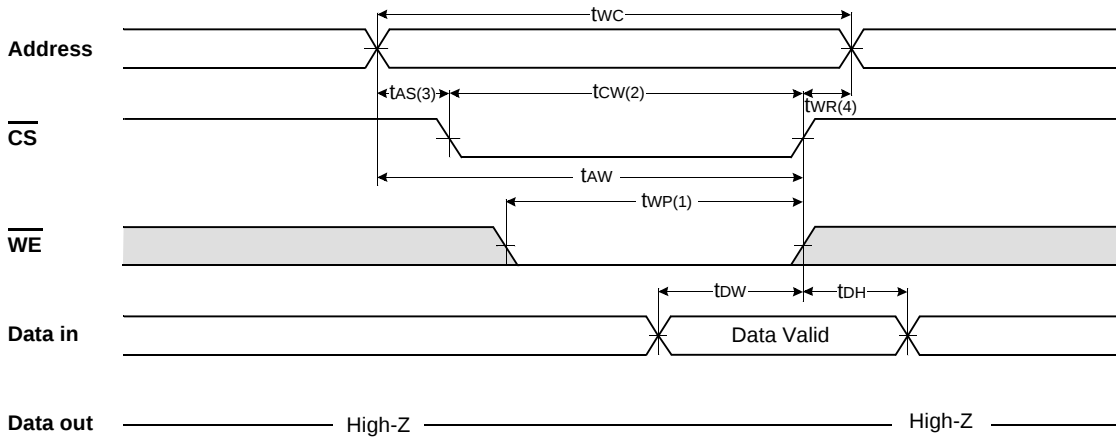
Item	Symbol	Test Condition		Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS} \geq V_{CC}-0.2\text{V}$		2.0	-	5.5	V
Data retention current	I _{DR}	$V_{CC}=3.0\text{V}, \overline{CS} \geq V_{CC}-0.2\text{V}$	K6X0808C1D-F	-	-	10	μA
			K6X0808C1D-Q	-	-	20	
Data retention set-up time	t _{SDR}	See data retention waveform		0	-	-	ms
Recovery time	t _{RDR}			5	-	-	

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

NOTES (READ CYCLE)

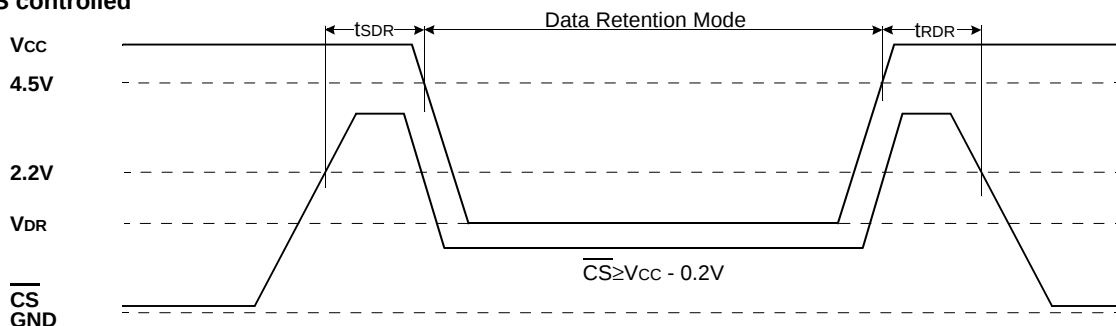
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)

NOTES (WRITE CYCLE)

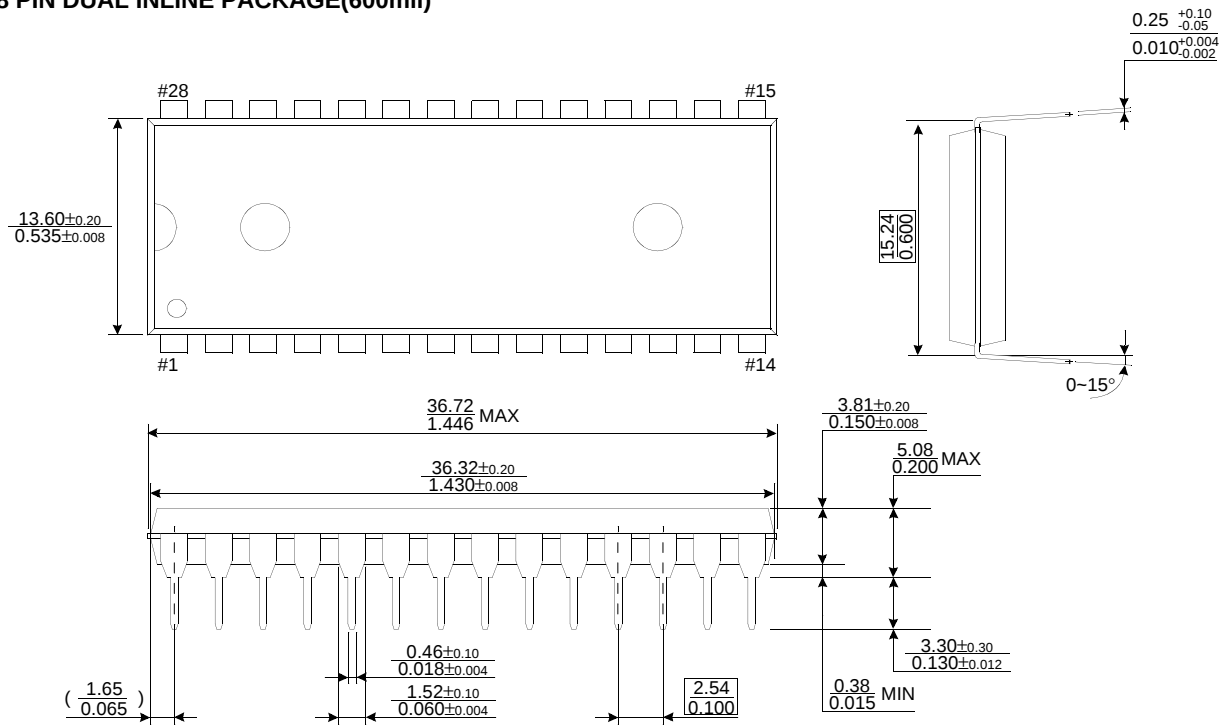
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going Low and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

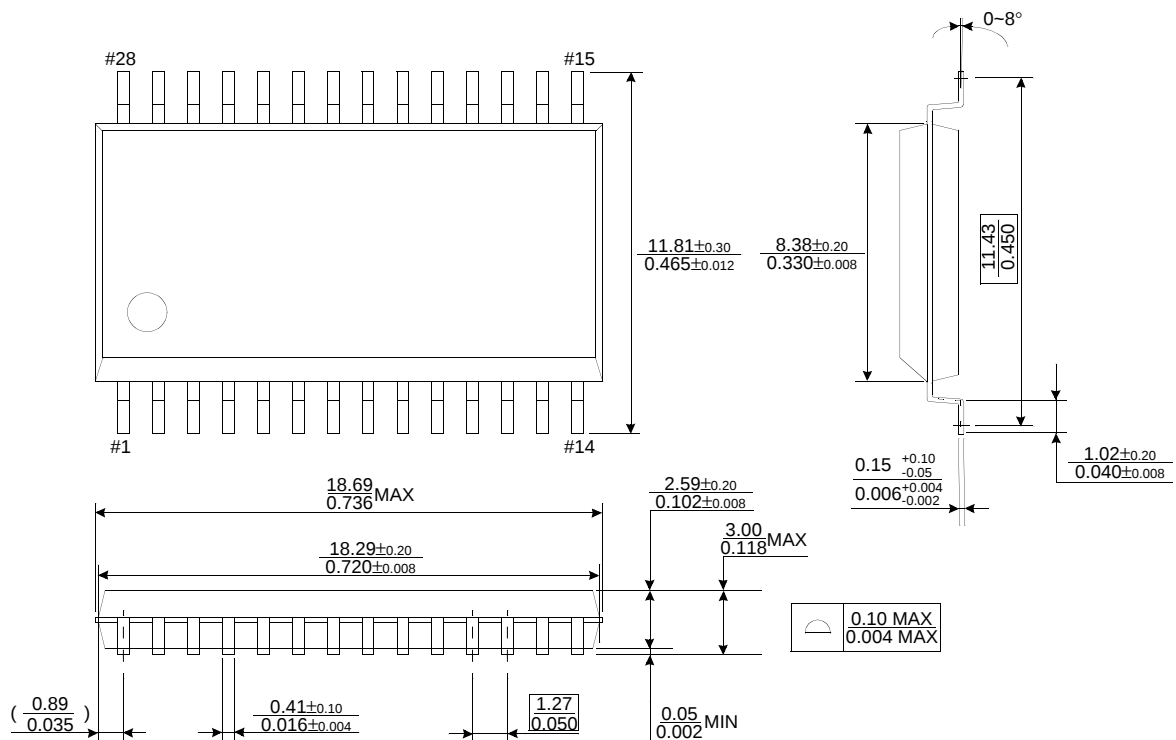
 $\overline{CS}$ controlled

Units: millimeter(inch)

3. FIN DUAL INLINE PACKAGE(00011111)



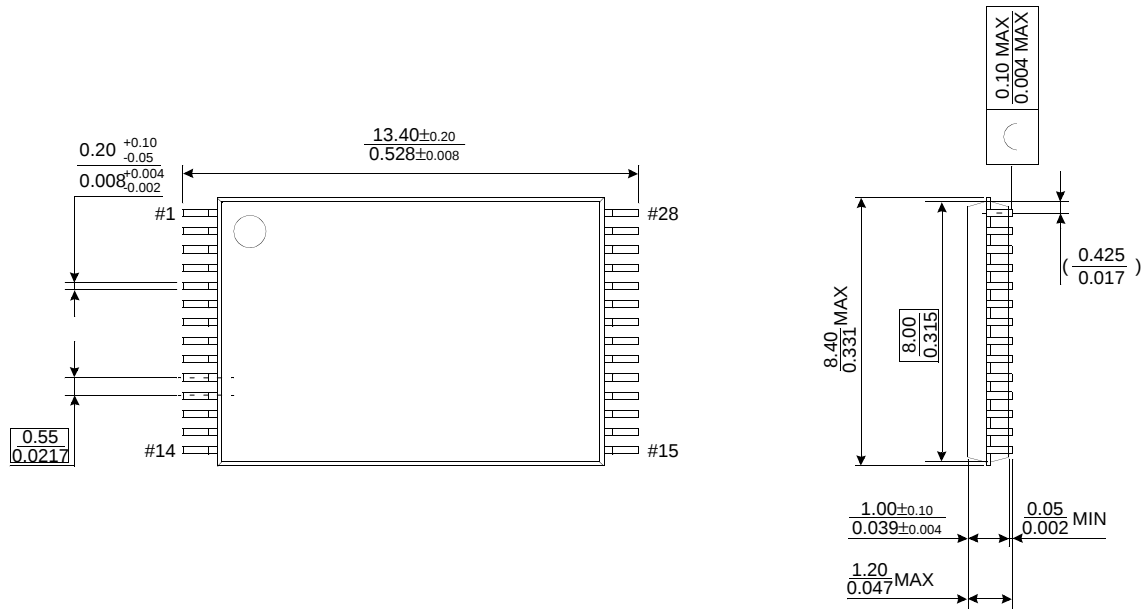
28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)



PACKAGE DIMENSIONS

Units: millimeter(inch)

28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)

